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DS, GS, AND DEPOT MAINTENANCE MANUAL

INTERROGATOR SET AN/TPX-50

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HEADQUARTERS, DEPARTMENT OF THE ARMY
AUGUST 1971

WARNING

DANGEROUS VOLTAGE EXISTS IN THIS EQUIPMENT

DON'T TAKE CHANCES !

EXTREMELY DANGEROUS VOLTAGES EXIST

IN THE FOLLOWING UNIT:

Receiver–Transmitter, Radio RT–903/TPX–50 1000 volts.

TECHNICAL MANUAL
NO. 11-5895-687-35-1

HEADQUARTERS
DEPARTMENT OF THE ARMY
WASHINGTON, D.C., *13 August 1971*

DS, GS and Depot Maintenance Manual
INTERROGATOR SET AN/TPX-50

			Paragraph	Page
CHAPTER	1.	INTRODUCTION	1-1—1-3	1-1
	2.	THEORY OF SIMILAR FUNCTIONS	2-1—2-5	2-1
	3.	IFF SYSTEM FUNCTIONING	3-1—3-7	3-1
	4.	CONTROL CIRCUIT FUNCTIONING	4-1—4-19	4-1
CHAPTER	5.	GENERAL MAINTENANCE INFORMATION		
Section	I.	Introduction	5-1—5-25	5-1
	II.	Tools and Test Equipment Required for DS, GS, and Depot Maintenance of Interrogator Set AN/TPX-50	5-26—5-27	5-20
CHAPTER	6.	TROUBLESHOOTING BASED ON STARTING PROCEDURE	6-1—6-5	6-1
CHAPTER	7.	CONTROL CIRCUITS TROUBLESHOOTING AND REPAIR		
Section	I.	Control Circuits Troubleshooting Information	7-1—7-2	7-1
	II.	Control Circuits Troubleshooting chart	7-3—7-6	7-4
	III.	Testing the control circuits	7-7—7-9	7-7
	IV.	Troubleshooting and Repair of Cabinet, Interrogator Set Group CY-6442/TPX-50.	7-10—7-13	7-7
	V.	Troubleshooting and Repair of Control, Interrogator Set C-7651/TPX-50	7-14—7-18	7-12
CHAPTER	8.	LAMP DRIVER CARD 2A1 TROUBLESHOOTING AND REPAIR	8-1—8-6	8-1
	9.	COMPLETE ALIGNMENT AND TESTING OF AN/TPX-50	9-1—9-3	9-1
	10.	GENERAL SUPPORT TESTING PROCEDURES (DELETED)		
	11.	DEPOT OVERHAUL STANDARDS	11-1—11-10	11-1
	12.	FOLDOUT DRAWINGS	12-1	12-1
APPENDIX		REFERENCES		A-1
INDEX				I-1

LIST OF ILLUSTRATIONS

Figure No.	*Title*	*Page*
2–1	Logic symbols used	2–3
5–1	Cables W1 and W2	5–10
5–2	Repair of coaxial cable RG–180	5–12
5–3	Hot mockup diagram for the IFF set	5–18
6–1	Interrogator group case power control panel, rear view	6–3
6–2	Control box panel, rear view	6–4
6–3	Interrogator group case, inside rear of group case, viewed through processor opening	6–5
6–4	Interrogator group case, power control panel and internal connectors	6–6
6–5	Troubleshooting waveforms	6–7
7–1	Filter panel, inside view	7–9
7–2	Connector panel, inside view	7–10
7–3	Interrogator group case, rear view panels removed	7–11
8–1	Lamp driver card 2A1	8–2
12–1	Color code markings for MIL–STD resistors and capacitors	12–3
12–2 ①	IFF set, system functional block diagram	12–5
12–2 ②	IFF set, system functional block diagram	12–7
12–2 ③	IFF set, system functional block diagram	12–9
12–3	IFF set, interconnection wiring diagram	12–11
12–4	Control circuits, functional block diagram	12–13
12–5	Interrogator group case unit 1, schematic diagram	12–15
12–6	Control box, interconnection block diagram	12–17
12–7	Lamp driver card 2A1, schematic diagram and component locations	12–19

CHAPTER 1

INTRODUCTION

1-1. Scope

a. This manual covers direct support, general support and depot maintenance for Interrogator Set AN/TPX–50 (IFF set). Chapters 3 and 4 cover functioning of the equipment; chapter 5 covers general maintenance information; chapters 6 through 9 cover troubleshooting, repair, removal and replacement of parts, and adjustment and alignment; chapters 10 and 11 cover general support testing procedures and depot overhaul standards; and chapter 12 contains all illustrations. TM 11–5895–687–12 covers installation, operation, and organizational maintenance.

b. Particular attention is paid in this manual to the following two units of the IFF set, other assemblies being more completely covered in separate manuals:

(1) Cabinet, Interrogator Set Group CY–6442/TPX–50 (interrogator group case).

(2) Control, Interrogator Set C–7651/TPX–50 (control box).

c. Reporting of errors, omissions, and recommendations for improving this publication by the individual user is encouraged. Reports should be submitted on DA Form 2028 (Recommended Changes to Publications) and forwarded direct to Commanding General, US Army Electronics Command, ATTN: AMSEL-MA-SR, Fort Monmouth, N.J. 07703.

NOTE

For applicable forms and records, refer to TM 11–5895–687–12.

1-2. Indexes and Publications

a. DA Pam 310–4. Refer to the latest issue of DA Pam 310–4 to determine whether there are new editions, changes, or additional publications pertaining to the equipment.

b. DA Pam 310–7. Refer to DA Pam 310–7 to determine whether there are modification work orders (MWO's) pertaining to the equipment.

1-3. General Information

a. The control box provides the asociated radar operator with all controls and indicators necessary for the operation of the IFF set. The interrogator group case provides the physical mounting and protective enclosure for the other assemblies: the synchronizer, processor, and receiver-transmitter.

b. The control box is used for power distribution, monitoring of equipment faults, and the selection of the operating modes for the associated equipment. The interrogator group case supplies all electrical power and signal connections for the assemblies it houses, plus provision for connections to external units with which the iff set operates.

c. Graphic symbols used on the illustrations in this manual are in accordance with those listed in MIL–STD–15–1A (Graphic Symbols for Electrical and Electronic Diagrams), MIL–STD–17 (Mechanical Symbols), and MIL–STD–806B (Graphic Symbols for Logic Diagrams).

d. Components of the IFF set that are mentioned frequently in this manual are usually referred to by their common names, which are listed in TM 11–5895–687–12.

e. Reference designations have been assigned to every unit and part in the equipment in accordance with the unit numbering method outlined in ASA 432.16 (1965) *American Standard Electrical and Electronics Reference Designations.* The number at the beginning of a reference designation denotes the unit in which the part is located. Each following letter-number combination, where included,

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Figure No.	Title	Page
2–1	Logic symbols used	2–3
5–1	Cables W1 and W2	5–10
5–2	Repair of coaxial cable RG–180	5–12
5–3	Hot mockup diagram for the IFF set	5–18
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6–3	Interrogator group case, inside rear of group case, viewed through processor opening	6–5
6–4	Interrogator group case, power control panel and internal connectors	6–6
6–5	Troubleshooting waveforms	6–7
7–1	Filter panel, inside view	7–9
7–2	Connector panel, inside view	7–10
7–3	Interrogator group case, rear view panels removed	7–11
8–1	Lamp driver card 2A1	8–2
12–1	Color code markings for MIL–STD resistors and capacitors	12–3
12–2 ①	IFF set, system functional block diagram	12–5
12–2 ②	IFF set, system functional block diagram	12–7
12–2 ③	IFF set, system functional block diagram	12–9
12–3	IFF set, interconnection wiring diagram	12–11
12–4	Control circuits, functional block diagram	12–13
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identifies, in order, the major assembly, the module, the printed wiring board or sub-assembly, and finally the component part, such as transistor, capacitor, or integrated circuit (IC). Paragraph 5–9 lists the reference designations assigned to each unit and major assembly in the IFF set and also gives an example of the breakdown of a reference designation into its basic parts.

f. The reference designations assigned to the interrogator group case and the control box are listed below.

Name	*Reference designation*
Interrogator group case	1
Control Box	2
Lamp driver board	2A1

g. Equipment panel markings are capitalized in text and are boxed on illustrations.

h. Broken lines on illustrations represent mechanical connections and solid lines represent electrical connections.

i. The physical locations of major components, modules, and operating controls of the IFF set; and removal and replacement procedures for major components and modules, are illustrated and described in TM 11–5895–687–12.

j. Coverage of the major assemblies of the IFF set, listed by their common names, is contained in the following manuals.

Assembly	*Manual No.*
Processor	TM 11–5895–687–35–2
Synchronizer	TM 11–5895–687–35–3
Receiver-transmitter	TM 11–5895–687–35–4

CHAPTER 2

THEORY OF SIMILAR FUNCTIONS

2-1. General

A number of similar functions are performed within the control box, unit 2, by the electronic circuits on lamp driver board 2A1 which light the green CHALLENGE lamp and the four red SELF TEST lamps. These circuits are represented on the functional block diagram (fig. 12–4) by logic symbols, rather than by rectangular blocks, to provide a clearer and more complete presentation of their functions and functional relationships.

2-2 Logic Symbols (fig. 2–1)

a. Logic symbols represent stages or circuits whose inputs and outputs are two-level signals. That is, each individual signal has only two possible voltage levels, high and low. The high level of a given signal is the higher or more positive of its two possible voltage levels, and is not necessarily the same as the high level of any other signal. Similarly, the low level of a given signal is its lower or less positive voltage level, and is not necessarily the same as the low level of any other signal. In all circuits on the lamp driver board, an open circuit at any input is equivalent to a high level of that input, and a ground at any input is a low input.

b. Each logic symbol indicates the response of a stage or circuit to one particular combination of input levels in such a manner that the response to any other combination of input levels can be deduced, and thus completely defines the function of the stage or circuit which it represents. The significant level of each signal is identified by the presence or absence of a small circle at the point where that signal is applied to or obtained from a logic symbol. The presence of a small circle designates the low level of a signal, and the absence of a small circle designates its high level.

2-3. Inverter Circuit

Symbol ① in figure 2–1 shows an inverter. This symbol consists of a triangle, which represents the amplifier function (also called the logical identity function), with a small circle at one, but not the other, of its two signal connections. In this case, with the small circle at the input, the stage or circuit is shown to deliver a high output, N, in response to a low input, A. Thus, by implication, the stage or circuit also delivers a low output in response to a high input. Both cases are indicated by the associated truth table in the figure.

2-4. AND Gate Circuits

a. Symbol ② in figure 2–1 shows a two-input AND gate. This symbol consists of the distinctive shape which represents the AND gate function, with no small circles at its inputs or output. The AND gate shape signifies that the indicated output level is obtained only if the indicated input levels are present simultaneously. In this case, the stage or circuit is shown to deliver a high output, N, only if both inputs, A and B, are simultaneously high. Thus, by implication, all other input combinations result in a low output, as indicated by the associated truth table.

b. Symbol ③ also shows a two-input AND gate, but with a small circle at input A. In this case, the stage or circuit is shown to deliver a high output, N, only if input A is low and input B is simultaneously high. Thus, by implication, all other input combinations result in a low output, as indicated by the associated truth table.

c. Symbol ④ shows another two-input AND gate, but with small circles at both inputs. In this case, the stage or circuit is shown to deliver a high output, N, only if both inputs, A and B, are simultaneously low. Thus by implication, all other input

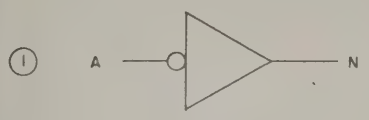
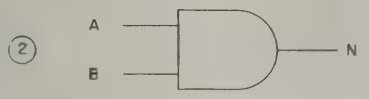
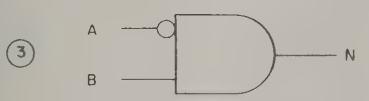
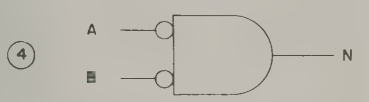
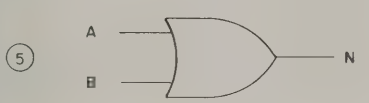
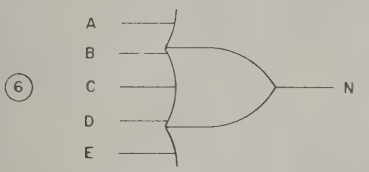
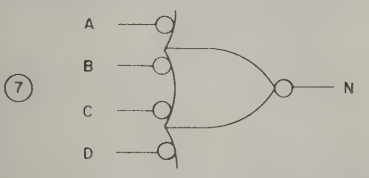
combinations result in a low output, as indicated by the associated truth table.

2-5. OR Gate Circuits

a. Symbol (5) in figure 2–1 shows a two-input OR gate. This symbol consists of the distinctive shape which represents the OR function, with no small circles at its input or output. The OR shape signifies that the indicated output level is obtained whenever any one or any combination of the indicated input levels is present. In this case, the stage or circuit is shown to deliver a high output, N, whenever input A is high, or input B is high, or both are high. Thus, by implication, the output is low only when both inputs are simultaneously low, as indicated by the associated truth table.

b. Symbol (6) shows a five-input OR gate which is similar to symbol (5) (no small circles) except for the number of inputs. In this case, the stage or circuit is shown to deliver a high output, N, whenever any one or any combination of its inputs, A, B, C, D, and/or E, is high. Thus, by implication, the output is low only when all five inputs are simultaneously low, as indicated by the associated truth table.

c. Symbol (7) shows a four-input OR gate with small circles at all four inputs and at the output. In this case, the stage or circuit is shown to deliver a low output, N, whenever any one or any combination of its four inputs, A, B, C, and/or D, is low. Thus, by implication, the output is high only when all four inputs are simultaneously high, as indicated by the associated truth table.

SYMBOL	LOGIC FUNCTION	TRUTH TABLE (INPUT COMBINATIONS & RESULTING OUTPUTS)
① 	INVERTER	A | N L | H H | L
② 	AND	A B | N H H | H L H | L H L | L L L | L
③ 	AND	A B | N L H | H H H | L L L | L H L | L
④ 	AND	A B | N L L | H H L | L L H | L H H | L
⑤ 	OR	A B | N H H | H L H | H H L | H L L | L
⑥ 	OR	A B C D E | N H * * * * | H * H * * * | H * * H * * | H * * * H * | H * * * * H | H L L L L L | L
⑦ 	OR	A B C D | N L * * * | L * L * * | L * * L * | L * * * L | L H H H H | H

NOTES:

1. H = HIGH (THE MORE POSITIVE OF THE TWO VOLTAGE LEVELS FOR A GIVEN INPUT OR OUTPUT)
2. L = LOW (THE LESS POSITIVE OF THE TWO VOLTAGE LEVELS FOR A GIVEN INPUT OR OUTPUT)
3. * = IMMATERIAL (MAY BE HIGH OR LOW WITH NO EFFECT ON OUTPUT N)

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Figure 2–1. Logic symbols used.

CHAPTER 3

IFF SYSTEM FUNCTIONING

3-1. General
(fig. 12-2)

a. This chapter describes the overall operation of the IFF system by discussing the interrelationship between the circuits of the interrogation group case, the control box, the processor, the synchronizer, and the receiver transmitter and references figure 12–2. Each rectangle, within the processor, synchronizer, and receiver transmitter blocks, represents a circuit which is discussed in detail in the manuals for those assemblies.

b. The following facts will be helpful in studying the block diagram discussion:

(1) All circled letters on signal functions refer to waveforms on the IFF set timing diagram, in TM 11–5895–687–12.

(2) Most rectangles on the block diagram, except for inverters and/or shapers, are identified by a name corresponding to a circuit in the assembly manuals.

(3) Although only the major signals are mentioned in this discussion, subordinate signals, except for clock pulses, are included on the block diagram to facilitate signal tracing.

3-2. Timing Circuits
(fig. 12–2)

The timing circuits (zone A9, fig. 12–2) of the IFF set receive a radar trigger through connector J1(A5) from the associated radar and generate four pretriggers, at precise intervals, to establish the necessary timing for each challenge-reply cycle.

a. Radar Trigger. Each radar trigger A initiates one challenge-reply cycle. The radar triggers are applied once for each sixteenth radar pulse repetition period (prp), and timed to occur 460 microseconds (μsec) before radar zero time. This establishes a pulse repetition frequency (prp) of 375 to 450 challenge-reply cycles per second, depending upon the prp of the associated radar.

b. Pretrigger Generation. The timing circuits, upon receipt of the radar trigger, provide five timing signals for synchronization of the functions of the IFF set. These timing signals, generated in a specific sequence, consist of four pretriggers (B) ; mode 4 pretrigger, self-test pretrigger, sif pretrigger, and processor start pretrigger; and a continuous 10–megacycle clock (10–mc clock) pulse train output. The radar trigger and all pretriggers are applied to the timing self-test circuit, which checks for the presence and correct sequence of those triggers.

(1) *Mode 4 pretrigger.* The mode 4 pretrigger is timed to occur 14.5 μsec after each radar trigger, (445.5 μsec before radar zero time). This pretrigger, after inversion and shaping by inverter shaper A1A7 (B9), is applied as follows:

(a) To the mode 4 enable and sync counting circuits (B10), the reply decoding self-test circuit (B14), the challenge self test circuit (B16), and the coder-decoder fault accumulator circuit (A17); for use in all modes as the pretrigger which marks the start of each prf.

(b) Through inverter A1A6 (C9) to the interrogator computer (E1), to initiate a challenge when operating in mode 4.

(2) *Self-Test Pretrigger.* The self-test pretrigger is timed to occur 340.0 μsec after the mode 4 pretrigger. This pretrigger is applied to the timing resetting circuits of the processor (A26) for use in all modes as a reset pulse which prepares the processor to start the processing of decoded replies in each prp. This same pretrigger, after inversion

through inverter A1A7 is applied directly to the challenge self-test circuit (B16), the interface fault accumulator circuit (E17), and through the pretrigger reshaping circuit (B10) to the delay line and delay line driver circuit (A11) and the reply decoding self test circuit (A14). This self-test pretrigger is used in all modes as the pretrigger which marks the start of synchronizer dead-time in each prp. It is during this dead-time that the synchronizer self-test cycle occurs.

(3) *Sif Pretrigger.* The sif pretrigger is timed to occur 395.2 μsec after the mode 4 pretrigger, and is used only within the synchronizer. This pretrigger is applied to the reply decoding self-test circuit (B14) to terminate each reply decoding self-test cycle and, during sif operation, is applied through the pretrigger reshaping circuit (B10) to the P1 and P3 trigger generation circuit (B13) to initiate sif challenge encoding.

(4) *Processor Start Pretrigger.* The processor start pretrigger is timed to occur 436.0 μsec after the mode 4 pretrigger, and is applied to the timing resetting circuit (A26) of the processor, as the pretrigger which initiates the processing of decoded replies in each prp. Within the synchronizer, this pretrigger is applied to the friend generation circuit (E20), the interface fault accumulator circuit (E17), the display gate generation circuit (D21), and to the test target generator circuit (C20) for use in all modes as the pretrigger which marks the beginning of reply processing.

(5) *10–Mc Clock Output.* The output of the 10-mc clock is a continuous pulse train which is applied to the challenge encoding and reply decoding circuits for the digitally timed functions that require a 10–mc clock rate within those circuits.

3-3. Mode Switching

(fig. 12–2)

Mode switching is accomplished by the settings of MODE SELECT switch S6(A3) and CODE SELECT switch assemblies A3(B4) through A12(B7) which are used in sif modes of operation (*a* below); and MODE SELECT switch S6 and MODE 4 switch S8(B3) which are used in mode 4 operation (*b* below). Modification of sif operation is accomplished by the setting of SIF REPLIES switch S7 (C6) (*c* below), while modification of sif and mode 4 operation is accomplished by the setting of PROCESSOR switch S4 (D6) (*d* below).

a. Sif Modes Switching. MODE SELECT switch S6A front, when set to 1, 2, or 3 A and with either CHALLENGE switch set to ON or with the input of an external challenge enable (A1), couples the selected mode enable (ground) to the selected CODE SELECT switch assemblies ((1) below) and to the sif enable generation circuit (A9) in the synchronizer ((2) below).

(1) The CODE SELECT switch assemblies are set to the code of the day for each sif mode of operation. When enabled, the selected code digit enables are applied through inverter A2A1 (E11) to the code pulse decoding circuit (E13). The code pulse decoding circuit uses these enables to recognize a correctly coded reply (para 3–5*b*) from the interrogated aircraft.

(2) Upon receipt of the selected sif mode enable the sif enable generation circuit provides the following.

(*a*) A mode 1, 2, or 3/A enable to the P1 and P3 generation circuit to enable the P1 tap output (18.0 μsec tap for mode 1, 15.95 μsec tap for mode 2, and 13.05 μsec tap for mode 3/A) and the P3 tap output (21.0 μsec) of delay line A5 (A11).

(*b*) An sif enable to the pretrigger reshaping circuit (B10) which also receives sif pretriggers from the timing circuits. The output of pretrigger reshaping circuits is a reshaped sif pretrigger which is applied to delay line A5 where it is used as the selected P1 and P3 pulses.

(*c*) An sif enable to the challenge self-test circuits (A16) for monitoring by the self-test circuits.

(*d*) An sif enable to the isls timing circuit (B17) which enables that circuit to generate an interrogation side lobe suppression (isls) (P2) pulse following the selected P1 pulse by 2.0 μsec.

(*e*) An sif enable to the target video selection circuit (D18) which, in turn, provides sif reply enables to the decoded reply and delayed video self-test circuit (D16) and to the target video reshaping circuit.

b. Mode 4 Switching. MODE SELECT switch S6A front (A3), when set to 4, TEST 4, or LOCKOUT OVERRIDE and with either

CHALLENGE switch S1 set to ON or with the input of an external challenge enable, couples a mode 4 enable (ground) to the mode 4 enable and sync counting circuit ((1) below) and to the interrogator computer ((2) below). MODE SELECT switch S6B front (B3), when set to TEST 4, provides a mode 4 test enable (ground) to the interrogator computer ((3) below). MODE SELECT switch S6B front when set to LOCKOUT OVERRIDE, provides a mode 4 noise alarm override (ground) to the interrogator computer ((4) below). MODE 4 switch S8A rear (C3) provides the computer with a mode 4 code A selection (open circuit) when set to A and a mode 4 code B selection (ground) when set to B; a refuel hold enable when set to CODE HOLD ((5) below); and a code zeroize control (ground) to relay K2 when set to ZERO ((6) below). MODE 4 switch S8A front, when set to CODE HOLD, provides a landing gear interlock signal (ground) to the interlock signal (ground) to the interrogator computer ((7) below).

(1) The mode 4 enable and sync counting circuit (B10) receives the mode 4 enable and, in turn, provides a mode 4 enable to the following circuits:

(*a*) Delay time sharing circuit (A10) where it is used to terminate challenge time 21.0 μsec after self-test pretrigger. Termination of challenge time initiates reply decoding time.

(*b*) Challenge video shaping circuit (B15) where it is used to enable the required circuits for reshaping mode 4 challenge video.

(*c*) Challenge self-test circuit (B15) where it is used to enable required circuits for mode 4 challenge testing.

(*d*) Triple pulse decoding circuit (D11) where it is used to enable the required circuits for decoding triple pulse replies.

(*e*) Isls timing circuit (B17) where it is used to enable required circuits for generation of the mode 4 isls trigger.

(*f*) Target video selection circuit (D18) where it is used to enable circuits which select the mode 4 decoded replies that are to be processed.

(2) The mode 4 enable enables the circuits of the interrogator computer to produce a mode 4 challenge whenever a mode 4 pretrigger is received.

(3) The mode 4 test enable enables circuits in the interrogator computer to provide, whenever a mode 4 trigger is received, a specially encoded interrogation for a specific aircraft.

(4) Whenever a low randomness condition is present in the encoding of mode 4 interrogations, a lockout is generated in the interrogator computer circuits and interrogations will cease. Upon receipt of a mode 4 noise alarm override the lockout is overridden and interrogations may be resumed.

(5) The refuel hold enable provides a mechanical hold to the mode 4 code whenever power is to be removed from the interrogator computer for more than 5 seconds.

(6) The code zeroize control causes relay K2 to energize, removing the ground from the zeroize return, which removes the electrical hold from the mode 4 code and causes it to zeroize.

(7) The landing gear interlock signal provides a mechanical hold to the mode 4 code as in (5), above.

c. SIF REPLIES switching. When operating normally in the sif modes of operation, SIF REPLIES switch S7 (C6) is in its spring loaded position (CODED). During this time, correctly coded sif replies are decoded and sif correct code video is applied through the target video selection circuit (D18) and target video reshaping circuit (D19) to the processor for processing and evaluation (para 3–5*c*). With SIF REPLIES switch S7 held to ALL, any sif reply containing correctly spaced F1 and F2 bracket pulses will be delivered as correct code video to the processor.

d. Processor Bypass Switching. During normal operation in any mode, PROCESSOR switch S4 (D6) is set to IN. During this time all decoded video is delivered to the processor for processing, and evaluations (para 3–5*c*). If a fault occurs in the processor, the CHALLENGE lamp DS1 (C6) will go out and PROC SELF-TEST (D6) lamp will light. In this event the processor may be bypassed by setting PROCESSOR switch S4 to BYPASS. This provides a processor bypass enable (ground) to lamp driver board 2A1 (D5) which will allow

CHALLENGE lamp DS1 to light when challenges are being transmitted. The processor bypass enable is also applied through inverter A1A2 (D9) to the target generation and processor bypass circuit (D20) and through inverter A1A8 (D21) to the iff video reshaping circuit (E21) and the target present (D16) and friend (E15) self test circuits. The bypass enable to these circuits permits all decoded video to be delivered directly and without processing to the associated radar as display video.

3-4. Challenging

(fig. 12–2)

During each challenge cycle a challenge is encoded in the selected mode of operation (*a*, below); an isls pulse is generated and inserted into the challenge video (*b*, below); the encoded challenge video is applied to the receiver-transmitter to modulate a 1030 mc signal to produce RF challenge pulses (*c* below), the RF isls pulse is removed from the RF challenge video and is transmitted through the difference RF channel and the RF challenge video is transmitted through the sum RF channel to the aircraft being interrogated.

a. Challenge Encoding. Generation of challenges in the sif modes of operation is a function of the synchronizer, while mode 4 challenges are generated within the interrogator computer. Each is enabled by the mode switching at the control box and challenges are initiated by respective pretriggers from the timing circuits in the synchronizer.

(1) *Sif challenge encoding.* When enabled for operation in one of the sif modes, the P1 and P3 trigger generation circuit (A13) receives the enabled sif pretrigger from the pretrigger reshaping circuit (B10). The sif pretrigger is applied through the delay line and delay line drive circuit as the trigger which is used to generate the selected sif challenge. The sif challenge consists of two challenge pulses, designated P1 and P3, separated by 3 μsec in mode 1, 5 μsec in mode 2, and 8 μsec in mode 3/A. The P1 pulse is taken from the delay line at the 18.0 μsec tap for mode 1, the 15.95 μsec tap for mode 2, and the 13.05 μsec tap for mode 3/A. The P3 pulse, which is timed to occur approximately 416.2 μsec after the mode 4 pretrigger, is taken from the 21.0 μsec tap. The sif (P1) trigger is applied to the isls timing circuit (B17) and to the challenge video shaping circuit (B15). Upon receipt of the P1 trigger the isls timing circuit generates, and applies to the challenge video shaping circuit, an sif isls (P2) trigger as an sif isls pulse which follows the P1 pulse by 2.0 μsec. The sif (P3) trigger is applied to the delay line time sharing circuit (A10) to set up that circuit to receive replies, and to the challenge video shaping circuit where it is inverted and applied through inverter A1A6 to the receiver-transmitter. The sif challenge video output (P1 and P3 challenge video pulses and the sif isls P2 pulse) of the challenge video shaping circuit is applied through inverter A1A6 (B18) to the receiver transmitter for transmission (*c* below).

(2) *Mode 4 challenge encoding.* When enabled for operation in mode 4, the interrogator computer receives the reshaped mode 4 pretrigger, encodes a mode 4 challenge, and generates a mode 4 gtc trigger. The mode 4 challenge consists of four sync pulses followed by a blank isls pulse space which, in turn, is followed by a coded challenge pulse train consisting of 21 to 32 pulses. The mode 4 challenge video is applied from the interrogator computer to the mode 4 enable and sync counting circuits (B10), the challenge video shaping circuit, and to the challenge self-test circuit. The mode 4 enable and sync counting circuit counts the four sync pulses and delivers the fourth sync pulse to the isls timing circuits (B17). The isls timing circuit generates a mode 4 isls trigger which is applied to the challenge video shaping circuit as a mode 4 isls pulse, 2.0 μsec after the fourth sync pulse. The mode 4 challenge video, which consists of the sync pulses and an isls pulse followed by a 21 to 32 pulse train, is applied through inverter A1A6 (B18) to the receiver-transmitter for transmission (*c* below). The mode 4 gtc trigger (E) from the interrogator computer, which is timed to occur shortly before the earliest possible mode 4 transponder reply pulse (373 μsec after the mode 4 pretrigger), is applied to the challenge self-test circuit (A15), and to the challenge video shaping circuit where it is inverted and applied through inverter A1A6 to the receiver-transmitter.

b. Isls timing. The isls timing circuit (B17) receives the sif P 1 trigger or the mode 4 4th sync pulse and the 10–mc clock pulses. A timing circuit, which is triggered by the sif pulse or by the fourth sync pulse and clocked by the 10–mc clock pulses, produces an isls gate and an isls trigger. The isls gate is timed to start 1.3 μsec after the input trigger and stop 2.7 μsec after the input trigger. The isls trigger is timed to occur 2.0 μsec after the input trigger. The sif isls (P2) trigger or the mode 4

isls trigger is applied to the challenge video shaping circuit where it is inserted into the challenge video. The isls gate is applied to the mode 4 enable and sync counting circuit to reset the counting circuits, and to the receiver-transmitter where it is used to switch the isls pulse out of the sum RF channel for transmission through the diff RF channel.

c. Challenge Transmitting. The receiver-transmitter receives the challenge video input and the isls gate from the synchronizer, generates modulation pulses and a 1030–mc excitation to produce RF challenge pulses, switches the RF isls pulse out of the sum channel, and transmits the RF isls pulse through the difference RF channel and the RF challenge pulses through the sum RF channel.

(1) The challenge video which is applied to modulation amplifier (E39) is amplified and applied to the cavity amplifier (E41) is XMTR MOD switch S3 is set to ON and if the 60 second fault control has elapsed.

(*a*) XMTR MOD switch S3 is provided for the use during maintenance and is set to OFF when the IFF set is receiving radar triggers, simulated or actual, and transmitting is not desired.

(*b*) The 60 second fault control prevents the challenge video output of the modulation amplifier for 60 seconds after power turn-on to provide a warmup period for the cavity amplifier. During this time a fault input is applied to the fault reset circuits (D42) which provide a receiver-transmitter fault enable to the control box.

(2) The cavity amplifier receives the amplified challenge video and the 1030–mc transmitter excitation and provides RF challenge pulses through the stripline coupler to the RF switch (D44).

(*a*) The transmitter excitation is originated in the 103–mc local oscillator and doubler. The 103–mc local oscillator is a crystal controlled Colpitts oscillator whose output is doubled to provide a 206–mc output to the frequency quintupler which, in turn, provides a 1030–mc transmitter excitation to the cavity amplifier and a local oscillator signal to sum and difference receiver circuits.

(*b*) The 1030–mc transmitter excitation is modulated by the amplified challenge video. The resultant RF challenge pulses are applied through the stripline coupler to the RF switch. The stripline coupler in conjunction with the receiver preselectors provides diplexing action which routes the RF pulses to the switch and not into the receiving circuits. In addition a detected transmitter output is provided to the transmitter fault detection circuits.

(3) The RF switch driver and performance monitor (E43) receives the isls gate from the synchronizer, provides the sum channel switch drive and diff channel switch drive to the RF switch, and an isls gate to the challenge monitor (E46).

(4) The RF switch receives the RF challenge pulses, the sum channel switch drive and the diff channel switch drive. The sum channel switch drive switches the RF challenge pulses to the stripline detector (D45) and the diff channel switch drive switches the isls pulse through the diplexer "T" to the difference antenna for transmission into the side lobes.

(5) The stripline detector receives the sum RF challenge pulses and passes them on to the sum antenna for transmission while detecting them for the challenge monitor which checks that the transmitter power is sufficient, and the voltage standing wave ratio (vswr) and, during the time of the isls gate, that the isls pulse is not present in the sum channel.

3-5. Reply Decoding
(fig. 12–2)

During each challenge-reply cycle, replies from transponders are received in the sum and difference antennas. Receiver circuits detect and compare the sum and difference replies, and route only sum receiver video to the synchronizer for decoding. Synchronizer circuits decode sif replies and mode 4 triple pulse replies. The interrogator computer receives the triple pulse decoded video from the synchronizer for time decoding and provides the synchronizer with mode 4 time decoded video. The decoded sif replies and mode 4 time decoded replies are applied to the processor for evaluation. After evaluation of replies, the processor provides the synchronizer with target or friend decisions which permit the synchronizer to route IFF display video to the associated radar set.

a. Receiving Circuits. The receiver receives the gtc trigger from the synchronizer, the gtc enable

from the control box, and the 1090–mc sum and diff receive RF from the antenna.

(1) The gtc trigger (B38), which is checked by the gtc trigger and receiver gate fault circuit (B39), is applied to the receiver gate generator to produce a receiver gate.

(2) The receiver gate, which is checked by the gtc trigger and receiver gate circuit, is applied to the video gating circuit (A47), the gtc control circuit (A38), and the self-test circuit (B39).

(*a*) The video gating circuit receives the receiver gate and allows receiver video to be sent to the synchronizer as long as the receiver gate is present. The receiver gate is of sufficient length to pass receiver video only for the full range of the IFF set.

(*b*) The gtc control circuit, enabled by the gtc enable and triggered by the leading edge of the receiver gate, generates and applies a time controlled threshold to the rsls video enable circuits (B47) where it is used for gtc processing (amplitude discrimination). Video signal amplitudes are compared against the time controlled theshold to determine if the amplitude of the video signal is appropriate for the time received.

(*c*) The self-test timing circuit uses the trailing edge of the receiver gate to start self-test time for the receiver-transmitter circuits.

(3) The 1090–mc sum and diff receive RF from the antenna are received through connectors J9 and J10 (D48), respectively. The sum receive RF is applied through the stripline detector, the RF switch, and the stripline coupler to the frequency converter, sum preamp, and IF log detector. The diff receive RF is applied through the diplexer to the frequency converter, diff preamp, and IF log detector. Each of these signals are heterodyned with the 1030–mc local oscillator signal to produce a 60–mc IF, and then amplified and applied through IF log detectors. The video output of the IF log detectors is logarithmically proportional to the input signal power. The sum video is applied to the video gating circuit (A47), the rsls video enable circuit, and the rsls comparator. The diff video is applied to the rsls comparator.

(*a*) The rsls comparator compares the sum and diff reply video to suppress replies whose amplitude indicates that the transponder is not in the sum lobe of the antenna, and provides a comparator pulse to the video gating circuit when it is determined that the transponder is in the sum lobe of the antenna.

(*b*) The rsls video enable circuit samples the comparator pulse and compares the sum video amplitude with the time controlled threshold. If both conditions are satisfactory, an rsls enable will be applied to the video gating circuit.

(*c*) The video gating circuit, enabled by the rsls video enable and the receiver gate, routes the sum video to the synchronizer for decoding and to the video fault circuits.

b. Decoding Circuits. The synchronizer receives transponder replies in the form of receiver video pulses from the receiver-transmitter. The receiver video is decoded in the delay line and, depending on the mode of operation, applied to the interrogator computer for further mode 4 decoding and/or for sif to the processor for processing and evaluation.

(1) *Sif Decoding.* Sif replies, in the form of receiver video pulses, are applied to the receiver video reshaping circuit (A14) where they are reshaped and applied as buffered receiver video to the delay line and delay line drive circuits (A11). A normal sif reply Ⓟ, Ⓢ, and Ⓥ consists of a combination of up to 12 code pulse (C1 through D4) contained between two bracket pulses (F1 and F2). The decoding circuits use the delay line to convert sif replies from serial form to parallel form for two types of decoding: bracket decoding and code pulse decoding. Either type of decoding may be used in the detection of i/p ⓆⓉⓌ and emergency ⓇⓊⓍ replies.

(*a*) Bracket decoding detects all sif replies by producing a single pulse for every pair of bracket pulses regardless of the code pulses contained between them. This is accomplished by enabling the (F2) 0.0 μsec and (F1) 20.3 μsec taps of the delay line. The simultaneous input of both pulses to the bracket decoding circuits provides: sif bracket decoded video to the reply decoding self-test circuits (B14); undelayed bracket decoded video to the i/p and emergency decoding circuit (D13) where it is used to decode emergency replies, and to the correct code pulse generation circuit (E13), where it is used in the generation of

a correct code pulse; and sif bracket decoded video to the decoded reply and delayed video self-test circuit (D16) where it is used during self-test time only, and to the target video selection circuit (D18) and the target video reshaping circuit (D19) where it is used, in both circuits, as correct code video.

(*b*) Code pulse decoding detects those code pulses present when the bracket pulses are at 0.0 μsec and 20.3 μsec taps of the delay line. All detected pulses are simultaneously applied to the code pulse decoding circuit (E13). The correct code is determined by the code digit enables, which are dependent on the setting of the selected CODE SELECT switches on the control box. If all expected code pulses are present, all unexpected code pulses are missing, and the bracket pulses are present, a C1–D4 go signal will be applied to the correct code pulse generation circuit. If these conditions are not met, a C1–D4 kill signal will be applied to the correct code pulse generation circuit.

1. Upon receipt of a C1–D4 go signal, the correct code pulse generation circuit provides: sif correct code video to the reply decoding self-test circuit (B14) where it is used during self-test time, and sif correct code video to the decoded reply and delayed video self-test circuit (D16) where it is used to check the decoded reply video, and to the target video reshaping circuit (D18) where it is used to generate decoded reply video, which is applied to decoded reply and delayed video self-test circuits, and to the reply processor for target or friend decisions.

2. Upon receipt of a C1–D4 kill signal, the correct code pulse generation circuit provides only a C1–D4 kill signal to the reply decodeing self-test circuit.

(*c*) I/p and emergency decoding detects bracket pulses and code pulses, as described in (1) and (2) above. Upon receipt of a normal sif reply, the i/p and emergency decoding circuit checks for the arrival (4.35 μs later) of an sp1 pulse to indicate an ident reply, or an F1 pulse of the first set of brackets which will indicate the arrival of an emergency reply. The decoded i/p or emergency reply is applied through the same circuits as that of a normal reply.

(2) *Mode 4 Decoding.* Mode 4 replies, in the form of receiver video pulses are applied to the receiver video reshaping circuit (A14), where they are reshaped and applied as buffered receiver video to the delay line and delay line drive circuit (A11). A Mode 4 reply Ⓖ consists of three pulses at 1.8 μsec intervals. The decoding circuits use the delay line to convert Mode 4 replies in serial form to parallel form. This is accomplished by enabling the 0.0 μsec, 1.8 μsec, and 3.6 μsec taps of the delay line. The triple pulse decoding circuit (D11) receives the coincident output of the triple pulse reply and provides the following.

(*a*) Triple pulse decoded video Ⓗ which after inversion through inverter A1A6 (D9) is applied as triple pulse decoded video to the interrogator computer. The interrogator computer time decodes the triple pulse video and applies Mode 4 time decoded video to the target video selection circuit (D18).

(*b*) Spoof counter video to the reply processor spoof counter register (B31) where it is used in the process of reply evaluation.

(*c*) Triple pulse decoded video and buffered 1.8 μsec, 3.6 μsec to the reply decoding self-test circuit.

c. Reply Processing. Reply processing consists of timing each reply into a range box which represents the position, in range, of the replying target; storing and counting replies for each prp in each range box; and, when the number of replies reaches a preprogramed count, supplying a target signal to the synchronizer; when the count increases above the target count to a higher preprogramed level, supplying a friend threshold signal followed by a friend signal to the synchronizer. The systems within the processor which are used for reply processing are: timing and control, memory, target arithmetic, and friend arithmetic.

(1) The timing and control system consist of the timing resetting circuits (A26) and 16–mc clock, and range box timing counter and decoders (C26). The timing resetting circuits (A26) receive the self-test pretrigger and provide: a reset X signal which resets the X–Y address counter (A27) and clocks the interrogation counter (D29); a reset which partially enables the self-test cycles counter (A30); and a reply lockout to the X–Y address counter, the reply limiter, and the timing counter and decoders. Approximately 96 μsec later the timing resetting circuits receive the processor start

pretrigger, remove the reply lockout, and provide a start reset pulse to the range box timing and decoders (C25) and to the timing error detector (B32).

(2) The start reset pulse resets the counters of the range box timing counter and decoders. These counters, which are clocked by 16–mc clock pulses, begin counting immediately and provide the necessary signals for reply processing. These signals, which are generated at 4 μsec intervals, are: the memory gate which is applied to the X–Y memory drivers (A28) where it is used to gate out the X and Y coordinates of each range box in the 17 plane memory (D28); the memory clock, which is applied to the memory address counter, occurs at the end of each range box to clock the memory address counter; the read, trigger, strobe, and write signals, in that order, are generated for each range box and are used virtually all of the processor circuits. The strobe signal is also delivered to the synchronizer for the gating of replies.

(3) The memory system consists of the X–Y address counter and X and Y memory drivers (A28) and the 17 plane memory (E28).

(4) The X–Y address counter generates X and Y counts which are decoded in the X and Y memory drivers. The X–Y counts are used to address memory locations of range boxes which represent the positions of replying IFF targets. These memory locations are in the 17 plane memory.

(5) The 17 plane memory (D28) is capable of storing 48 data bits in each of its 17 planes, one data bit for each range box. Memory planes 1 through 4 store the interrogation count, planes 5 through 10 the friend count, plane 11 the friend identification bit, plane 12 the odd/even bit, plane 13 the target present bit and planes 14 through 17 the target count. Data is read out of memory during read pulse time to the target and to the friend arithmetic systems. The data is then updated and written into memory during write pulse time.

(6) The reply limiter circuit permits reply signals to be gated through the range box reply zone register at 4 μsec intervals, preventing more than one reply in a given range box. The circuits of the range box reply zone register and decodes, the odd/even decoder, and reply flip-flop assign each reply to an appropriate range box in memory.

(7) The target memory register (E28) receives the old target count from memory planes 14 through 17. This count applied to the target adder as the augend and to the add/subtract control to develop the addend for the target adder. The addend is a +2 if a reply has been received and a -1 if no reply is present.

(8) The target adder receives th augend from the memory register and the addend from the add/subtract control. The resultant count is applied to the target start decoder, the new target count gating circuits, and to the target end decoder.

(9) The target arithmetic system consists of the reply discriminator and the target arithmetic circuits. The reply discriminator circuits consist of the reply limiter (B27); and the range box reply zone register and decoders, odd/even decoder, and reply flip-flop (D27). The target arithmetic circuits consist of: the target memory register, add/subtract control and target adder circuits (E28); the target start decoder (D32); the target present gating (D33); the target present flip-flop (D30); the new target count gating circuits (C33), the friend trigger gating circuit (D33), and the target end decoder.

(10) The target start decoder decodes the input from the target adder in each range box and if the new target count equals or exceeds the target start threshold, a target start pulse will be generated at write pulse time. The target start pulse is applied to the new target gating, the friend threshold detector (E36) and friend adder and friend threshold decoder (E35).

(11) The target present gating circuit receives target start and target for a given range box. As long as these two signals are present a one is written into memory plane 13 at write pulse time.

(12) The target present flip-flop is set during each prp in which target start is reached in a given range box and continues to be set for that range box until target end is reached. Its purpose is to recirculate the target present bit from memory plane 13 and to supply target to the synchronizer.

(13) The new target count gating circuits receive the friend trigger and gate the new target count from the target adder into memory planes 14 through 17 at write pulse time for each range box.

(14) The target end decoder samples the new target count from the target adder during each range box and generates a target end signal when the count drops below a preprogrammed level. The target end signal is applied to target present gating and friend present gating circuit (D34).

(15) The friend trigger gating circuit generates a friend trigger in every range box regardless of whether or not a target is present and continues to do so until target end is reached. When target end is reached in a range box, the loss of the friend trigger pulse causes all zeros to be written into memory for that range box. The friend trigger is applied to the new target count gating circuits, friend identification flip-flop and friend bit decoder (C35), and friend output circuit (C36).

(16) The friend arithmetic system consists of the spoof counter circuits, the interrogation counter (D29), and the friend arithmetic circuits. The spoof counter circuits consist of the spoof counter shift register (B31) and the spoof counter up–down counter (B30). The friend arithmetic circuits consist of friend weighting circuits (E30), friend register (D34), friend adder and friend threshold, decoder (E34), threshold detector, friend identification, flip-flop and friend bit decoder (C35), and friend output circuit (C36).

(17) The spoof counter, which consists of the spoof counter up/down counter (B30) and spoof counter shift register (B31), receives the spoof counter video from the synchronizer. These circuits record the time-undecoded replies (spoof counter video pulses). The stored count is applied to the friend weighting circuits (E30) where it is used to determine the weight (value of count) to be added to or subtracted from the friend count.

(18) The interrogation counter counts the number of interrogations for each range box in which a target bit is present. If a preprogrammed upper limit is reached, an interrogation limit is applied to the friend weighting circuits to inhibit friend up-counting.

(19) The friend weighting circuits decode the spoof count for each range box and cause weighted counts to be added to or subtracted from the friend count. Addition occurs if a reply is present in a given range box and subtraction if no reply is present. The add/subtract count is applied to friend adder and friend threshold decoder circuits.

(20) The friend register receives the old friend count for each range box from memory planes 5 through 10 and applies this count to the friend adder and friend threshold decoder circuits.

(21) The friend adder receives a friend count from the friend register and and add/subtract count from the friend weighting circuits and provides a new friend count to the friend threshold decoder and to the friend output circuits. When the new friend count reaches a preprogrammed count friend threshold is applied to the friend threshold detector and to the friend identification flip-flop and friend bit decoder.

(22) The friend threshold detector receives the friend threshold from the friend threshold decoder and applies a friend threshold to the synchronizer.

(23) The friend bit decoder generates a friend bit for storage in memory in a range box in which a reply has been received or the new friend count exceeds a preprogramed number and a target is present, a friend trigger is available and friend threshold has been reached. This bit is recirculated into memory for that range box as long as there is a target present and a friend trigger is available.

(24) The friend identification flip-flop provides a friend signal to the synchronizer one prp after friend threshold has been reached in a given range box. This signal continues for that range box until one prp after target end.

(25) The friend output circuit gates the new friend count for each range box from the friend adder into memory planes 5 through 10 at write pulse time. Friend counting gating starts when interrogations start and continues until target end.

d. Iff Display Video. Selection of the reply video, for which the processor has supplied target, friend threshold, or friend, as IFF display video is a function of the display video interface circuit. This circuit receives the decoded sif correct code video, and the Mode 4 time decoded video and delivers decoded reply video to the processor. This same reply video is delayed within display video interface circuits for 5 μsec to allow the processor time for evaluation of the reply and for synchronization of the IFF display video with the radar return from the IFF target. The circuits of the display video circuit which are used to deliver target and friend

pulses to the associated radar as IFF display video are: the target video selection circuit (D18), the target video reshaping circuit (D19), the digital delay circuit (E19), the friend generation circuit (E20), IFF video shaping circuit (E21), and the display gate generation circuit (D21).

(1) The target video selection circuit receives the sif correct code video and the sif bracket decoded video during sif operation and Mode 4 time decoded video during mode 4 operation. The selected target video is applied as target line input to the target video shaping circuit and to the decoded reply and delayed video self-test circuit.

(2) The target video reshaping circuit reshapes the target line input and provides decoded reply video to the processor (*b* (1) (*b*) above) and undelayed target video to the digital delay circuit.

(3) The digital delay circuit delays the undelayed video for 5 μsec and provides delayed target video to the decoded reply and delayed video self-test circuit; and delayed target video to the friend self-test circuit, the target present self-test circuit, target generation and processor bypass circuit, and the IFF video reshaping circuit.

(4) During sif operation, when the processor decision is target, target is applied from the processor through inverter A1A8 as target gated and target gated to the target generation and processor bypass circuits. This circuit also receives the delayed target video pulse for which target has been supplied. The resultant output is a target present trigger to the IFF video shaping circuit, where it is reshaped to a nominal 1.0 μsec with a nominal amplitude of 3.0 volts and delivered to the associated radar as IFF display video.

(5) During mode 4 operation, when the processor decision is target, the operation is the same as for sif. However, when the processor decision is friend threshold, or friend, friend threshold or friend is applied to the friend generation circuit which provides a friend stored level to the IFF video shaping circuit. The video shaping circuit reshapes the delayed target video pulse to a nominal width of 5 μsec and a nominal amplitude of 5.0 volts for delivery to the associated radar as IFF display video.

3-6. Self-Test Circuits and Fault Indicators (fig. 12–2)

Self-test circuits are contained in each of the assemblies of the interrogator group. These circuits monitor operation of the IFF set, during each challenge reply cycle. If these circuits detect faulty operation of the IFF set, FAULT indicators will be lighted on the faulty assembly, a SELF TEST fault indicator on the control box will be lighted for the faulty assembly, and a remote error indicator enable will be supplied to the associated radar to indicate an IFF set fault.

a. Synchronizer Self-Test Circuits and Fault Indicators. During operation of the IFF set, self-testing is performed in the timing circuits, the challenge encoding circuits, the reply decoding circuits, and the display video interface circuits of the synchronizer.

(1) *Timing circuits self-test.* The timing self-test circuit (fig. 12–1, zone A10) monitors the prf of the radar trigger (A) input, from the associated radar, and the generation and sequence of the four pretriggers (B) . If the radar trigger prf is less than 200 or more than 625 triggers per second a radar trigger fault will be delivered to the fault driver circuit (B18) which lights RADAR TRIGGER FAULT indicator DS1 (B18). At the same time a radar trigger fault is delivered to the coder-decoder fault accumulator (B17) where it is used to prevent any other fault signals to be delivered to the fault driver circuits. During pretrigger generation the timing of the pretriggers is monitored. If any pretrigger occurs too frequently, if it does not occur at all, or if it occurs out of sequence, a timing fault will be delivered to the fault driver circuit which lights TIMING FAULT indicator DS2, SYN SELF TEST fault indicator DS5 on the control box, and provides a remote indicator enable to the associated radar.

(2) *Challenge encoding circuit self-test.* The challenge self-test circuit (B16) monitors signals generated by the challenge encoding circuits. During sif operation in each prp, this circuit checks for the generation of one, and only one, P1 challenge video pulse after the self-test pretrigger; one, and only one, isls gate after the P1 pulse; an isls P2 pulse within the isls gate, if the isls pulse is not being inhibited; a gtc trigger after the isls gate; and

one, and only one, P3 challenge video pulse. During mode 4 operation, in each prp, this circuit checks for one, and only one, fourth sync pulse; a challenge video pulse coincident with the fourth sync pulse; one, and only one, isls gate occurring after the fourth sync pulse and before the first challenge pulse; and one and only one gtc trigger if it is not inhibited from the R/T. If any expected input to the challenge self-test is missing in sif, an sif fault will be delivered to the coder-decoder fault accumulator circuit, if more than one pulse (P1, P2, P3, or mode 4 isls) is generated an excess pulse fault will be delivered to the coder-decoder fault accumulator circuit, or if any of the mode 4 sync pulses are not present a mode 4 fault will be delivered to the coder-decoder fault accumulator circuit. The coder-decoder fault accumulator circuit provides a coder-decoder fault output to the fault driver circuit if fault signals are received in two of three successive prp. This fault signal lights CODER-DECODER FAULT indicator DS3, SYN SELF TEST fault indicator on the control box, and provides a remote error indicator enable to the associated radar.

(3) *Reply decoding circuits self-test.* The reply decoding self-test circuit (B14) tests the sif and mode 4 decoding circuits after every radar trigger whether the IFF set is challenging or not. The decoding self-test cycle is initiated by each self-test pretrigger. The reply decoding circuits check that the triple pulse decoding circuit provides a triple pulse decoded video pulse in response to a mode 4 reply; the sif reply decoding circuit provides an sif correct code pulse and bracket decoded video in response to a correctly coded sif reply; the sif reply decoding circuits are capable of producing a kill pulse for an incorrectly coded sif reply; and the delay line drive circuit has functional continuity to the 0.00 μsec delay line input and through the delay line to every tap used for reply decoding. If all four conditions are not verified the cycle ends with a decoding fault input to the coder-decoder fault accumulator, with the same results as for the challenge fault in (2) above.

(4) *Display video interface circuit self-test.* The display video interface self-test circuits consist of the decoded reply and delayed video self-test circuit, the target present self-test circuit, and the friend self-test circuit. When the IFF set is receiving replies, these circuits monitor the passage of reply signals through the display video interface circuit.

(*a*) The decoded reply and delayed video self-test circuit monitors the operation of the target video selection circuit, target video shaping circuit and the digital delay circuit. If the sif correct code video or the mode 4 time decoded video is not selected, reshaped, and correctly delayed a decoded reply fault or delayed video fault will be applied to the interface fault accumulator. The interface fault accumulator circuit provides an interface fault output to the fault driver circuit if fault signals are received in two of three successive prp. This fault signal lights INTERFACE FAULT indicator DS4, SYN SELF TEST fault indicator DS5 on the control box and provides a remote indicator enable to the associated radar.

(*b*) The target present self-test circuit monitors the operation of the target generation circuit (D20). If the target generation circuit does not produce a target present trigger in response to each delayed video pulse for which the processor supplies target or if it does not provide a target present trigger for every delayed target video pulse when the processor is being bypassed, a target present fault will be applied to the interface fault accumulator circuit with the same result as for decoded reply fault in (*a*) above.

(*c*) The friend self-test circuit monitors the operation of the friend generation circuit (E20). This circuit is self-tested only during mode 4 operation. If the friend generation circuit does not produce a friend stored pulse for each delayed video pulse for which the processor has supplied friend threshold or friend, a friend fault signal will be applied to the interface fault accumulator with the same results as for decoded reply fault in (*a*) above.

b. Receiver-Transmitter Self-Test Circuits and Fault Indicators. During operation of the IFF set, self-testing is performed in the transmitting and receiving circuits of the receiver transmitter. These tests are performed for 50 μsec following the end of the receiver gate.

(1) *Transmitting circuit self-test.* Self-Test of the transmitting circuits is performed by the transmitter/power supply fault circuits (D41) which monitor the RF challenge pulses and the power supply voltages the RF switch driver/performance monitor (E43) which checks the operation of the RF switch (E44), and the challenge monitor (E46) which checks for the presence of an isls pulse in

the sum channel, the voltage standing wave ratio (vswr), the transmitted detected power, and the reflected detected power.

(*a*) The transmitter/power supply fault circuits (D41) are enabled by the modulation pulses and check for an RF challenge pulse for each modulation pulse received. If the RF challenge pulses are not of sufficient amplitude or if they are missing, a transmitter/power supply fault is generated. This signal lights XMTR FAULT lamp DS3 (C44) and is applied to the fault reset circuits (D42). The fault circuits provide a receiver-transmitter fault indicator enable to the control box to light R/T SELF TEST fault indicator DS9 and to provide a remote error indicator enable to the associated radar.

(*b*) The RF switch driver/performance monitor (E43) checks the RF switch for short or open RF switch diodes. If a short or open is detected, an RF switch fault is generated. This signal lights RF SWITCH FAULT lamp DS3 and is applied to the fault reset circuits with the same results as in (*a*) above. At this time an isls pulse inhibit is delivered to the synchronizer, to prevent isls (P2) pulse generation and to the control box where it is used to permit challenging when the R/T SELF TEST fault indicator lamp is lit (para. 4–17*b*).

(*c*) The challenge monitor circuit checks for the presence of isls gates, sufficient power output, acceptable vswr, and for the absence of the isls pulse form the sum channel. If any of these conditions are unsatisfactory, the challenge monitor enable to the control box will be removed and the CHALLENGE lamp will go off (para 4–17*c*).

(2) *Receiving circuit self-test.* Self-testing of the receiver circuit is accomplished by enabling the fault circuits with the challenge video, resetting the fault circuits with the gtc trigger and testing the receiver with a simulated target reply. This is a function of the gtc trigger and receiver gate fault circuit (B39), the rsls self-test circuit (B46), the receiver/rsls fault circuit (C41), the video fault circuits (D41), and the fault integrating circuits (B40).

(*a*) The gtc trigger and receiver gate fault circuits are enabled by the gtc trigger to expect the input of a receiver gate. This same gtc trigger is applied as a reset trigger to the fault reset circuits (D42) which, in turn, provide a reset pulse to the fault circuits. If the receiver gate is not received a receiver gate fault is applied to the video fault circuits ((*f*) below).

(*b*) The trailing edge of the receiver gate, which signifies the end of receiver time for each challenge reply cycle, is applied to the self-test timing circuit (B39). This circuit generates a 50 μsec self-test gate which is applied to the fault circuits to indicate self-test time and to the self-test modulation regulator (B41). The modulation regulator generates a trigger which is applied to the self-test of signal generator circuit (B42). This circuit generates a 218–mc self-test RF which is amplitude controlled by the signal generator trigger. The 218–mc RF is multiplied five times to a1090–mc self-test signal by the frequency quintupler (B43). The 1090-mc self-test signal is applied to the sum and diff frequency converter, preamp, and log IF detector circuits as with sum and diff receive RF. The sum video output is applied to the video gating circuit (B47), to the rsls self-test circuit (B46), and to the receiver/rsls fault circuits ((*d*), below). The diff video output is applied to the rsls comparator (C47) and to the rsls self-test circuit where it is compared with the sum video input to that circuit.

(*c*) The rsls self-test circuit compares the sum video and diff video inputs. If these signals are equal in amplitude a favorable rsls go/no–go signal is applied to the receiver/rsls fault circuit. If these signals are not equal in amplitude a nonfavorable rsls go/no–go signal is applied to the receiver/rsls fault circuit ((*e*) below).

(*d*) The video gating circuit receives a 4 μsec receiver gate 20 μsec after the start of the self-test gate. This 4 μsec gate permits the video gating circuit to provide a 4 μsec receiver video pulse to the video fault circuits (where it is checked for amplitude).

(*e*) The receiver/rsls fault circuits are enabled by the challenge video and reset by the gtc trigger. During self-test time, these circuits check the sum video amplitude and the rsls go/no–go input. If either signal is not as it should be, a detected fault is applied to the fault integrating circuit (B40) ((*g*) below).

(*f*) The video fault circuits are enabled by the challenge video and reset by the gtc trigger. During self-test these circuits check the receiver

video. If the receiver video is not of sufficient amplitude or if it is missing, a detected fault is applied to the fault integrator circuit.

(*g*) The fault integrating circuit receives a one μsec fault sample pulse during the 23rd μsec after start of the self-test gate. Any fault being applied at that time from any of the fault circuits will be registered in the fault integrating circuit. Several detected faults are required to provide an integrated fault signal to the fault circuits. Any fault circuits containing a fault at that time will cause a FAULT indicator to light.

(*h*) If the receiver/rsls circuits contain a fault when an integrated fault is received, a receiver/rsls fault will light RCVR FAULT lamp DS2, and will be applied to the fault reset circuit (D42). If the video fault circuits contain a fault when an integrated fault is received, a video fault will light RCVR FAULT lamp DS2, and will be applied to the fault reset circuit. If the transmitter/power supply fault circuits contain a fault when an integrated fault is received, a transmitter/power supply fault will light XMTR FAULT lamp DS3 and will be applied to the fault reset circuit.

(*i*) Upon receipt of a fault input, the fault reset circuit delivers to the control box, a receiver-transmitter fault indicator enable which lights R/T SELF-TEST fault indicator DS9, and is delivered to the associated radar as a remote fault indicator enable.

c. Processor Self-Test Circuits and Fault Indicators. During operation of the IFF set, self-testing is performed in timing circuits, memory circuits, and target and friend arithmetic circuits. The self-test circuits consist of the timing error detector (B32), the self-test cycle counter and decoders (A30), the self-test reply and error gates (A31), and the error indicator drivers (A33).

(1) *Timing error detector.* During the first range box of each prp, the timing error detector checks for the presence of the start reset, read, trigger, strobe, and write pulses. If, during this time, one of the pulses are missing or is generated out of sequence a timing error will be applied to the self-test and error gates and a timing error will be applied to the error indicator devices. The timing error prevents the self-test and error gates from generating a fault output for a fault that could be the result of a timing error. The timing error applied to the error indicator drivers results in the lighting of TIMING FAULT lamp DS1 and a processor fault indicator enable is delivered to the control box to light PROC SELF TEST fault indicator DS8, and is delivered to the associated radar as a remote indicator enable to indicate an IFF set fault.

(2) *Self-test cycle counter and decoders.* At read pulse time, when the address of range box 48 (X8–Y8) occurs, a self-test signal is generated in the self-test cycle counter and decoders. This signal is used extensively throughout the processor and is applied as processor self-test gate to the synchronizer to inhibit the input of reply video during self-test time. This circuit also generates eight additional gating signals which are generated for specific cycles of the 63 cycle self-test period. These gating signals are: cycle 0/1, cycle 2, cycle 3 and last cycle which occur at fixed times; and target gate, friend gate, undecoded reply gate which are programmable.

(3) *Self-test reply and error gates.* The self-test reply and error gates test the memory circuits and produce simulated triple pulse and time decoded replies to test the target arithmetic and friend arithmetic circuits.

(*a*) *Memory self-test.* The self-test reply and error gates circuit check the memory circuits during self-test cycle 0/1, 2, and 3. During cycle 0/1, a 17 bit message, consisting of all ones, is written into the 17 planes of memory. These bits are read out during the strobe pulse time of cycle 2 and compared to the input. If the bits read out of memory do not agree with those written in, a memory fault is registered in the self-test reply and error gates circuit and self-testing terminated until the next prp. If a memory fault is registered for any three consecutive prp a memory error and an error gate will be generated and applied to the error indicator drivers ((4) below). At write time of cycle 2 a 17 bit message consisting of all zeros is written into the 17 planes of memory and read out and checked as outlined above.

(*b*) *Target arithmetic and friend arithmetic circuits test.* The self-test reply and error gates generate simulated triple pulse decoded replies, gated by the undecoded reply gate, and time decoded replies, gated by the decoded reply gate at strobe time, in preprogrammed self-test cycles following cycle 3. The triple pulse decoded replies

(spoof counter video) are applied to the spoof counter shift register (B31) and the time decoded replies (self-test reply) are applied to the reply limiter. As the number of replies increase in the target arithmetic circuits a target signal is applied to the self-test reply and error gates circuit. A further increase in the number of replies results in a friend signal, from the friend arithmetic circuits, being applied to the self-test and error gates. If the arrival of target and friend coincides with the input of a target gate and friend gate input, respectively, from the self-test cycle decoder, the target arithmetic circuits are functioning properly. If, however, a target signal is received without a target gate and vice versa, a target error will be registered in the self-test reply and error gates circuit and self-testing will be terminated until the next prp. If target errors are detected in three consecutive prp a target error and a target gate will be applied to the error indicator drivers. If a friend signal is received without a friend gate and vice versa the action is the same as for the target signals, except that if friend faults are detected in three consecutive prp friend error and an error gate will be applied to the error indicator drivers.

(4) *Error indicator drivers.* The error indicator drivers receive the memory error, target error, and friend error, each of which is provided with an error gate. A memory error lights MEMORY FAULT lamp DS2, a target error lights TARGET FAULT lamp DS3, and a friend error lights FRIEND FAULT lamp DS4. Any error received by the error indicator drivers results in a processor fault indicator enable signal being applied to the control box where it lights PROC SELF TEST fault indicator DS8 and is applied as a remote error indicator enable to the associated radar to indicate an IFF set fault.

3-7. Test Target Mode

(fig. 12–2)

Operation in the test target mode provides the associated radar with a visible check of the processor's ability to process friend replies and of the synchronizer's ability to generate IFF display video in response to the processor decisions. During this mode, friend IFF display video is supplied for each of the active range boxes. This is accomplished by the generation of simulated mode 4 replies (test target video pulses) which are passed through the circuits of the processor and the synchronizers display video interface circuit to become IFF display video. The test target video pulses are generated in 16 groups with the pulses in each group spaced 16 range boxes apart and with the pulses in each group one range box greater in range than the corresponding pulses in the preceding group. Each complete cycle of 16 consecutive groups of tests target video pulses simulates individual decoded mode 4 replies in all active range boxes.

a. When CHALLENGE switch S1 (A2) on the control box is held to TEST, a test target enable is applied through inverter A1A2 (C9) as test target enable to the target video reshaping circuit (D19) and to the test target generator circuit (B20). The test target generator which is enabled by the test target enable and triggered by the processor start pretrigger receives and counts strobe pulses from the associated radar. After the input of the processor start pretrigger, a target video pulse is generated for every sixteenth strobe pulse input until the processor self-test gate is received. This is repeated 32 times, at the same ranges, to allow the processor to reach friend decisions in those range boxes. For the next 32 processor start pretriggers no test targets are generated which completes the first cycle. This cycle is repeated 15 more times in succession with each set of replies occurring one range box (one strobe pulse) greater in range.

b. Test target video pulses are processed in the same way as mode 4 replies (para 3—6). The resultant IFF display video at the associated radar is a spiraling display of friend reply video.

CHAPTER 4

CONTROL CIRCUIT FUNCTIONING

4-1. General

The control circuits for the IFF set are contained in the control box and in the power control panel, which is located on the interrogator group case. Power circuit breakers on the processor, synchronizer, and receiver-transmitter, which are normally in the ON position, are not involved in the normal operation of the system.

4-2. Control Circuits
(fig. 12–3)

a. The control circuits serve two primary purposes:

(1) When turning the IFF set on, they provide for the distribution of power to all units of the set and to the interrogator computer.

(2) They provide for control and monitoring of all functions connected with the operation of the IFF set. Control and monitoring is accomplished by the use of switches and indicator lamps.

b. The control functions are discussed in paragraph 4–3, in the order of first use during normal operation, after all initial control settings have been made at the other assemblies of the IFF set. Normal operation consists of five basic procedures:

(1) Turning on the IFF set, which covers power distribution.

(2) Performing confidence checks.

(3) Preparing to challenge.

(4) Challenging.

(5) Turning off the IFF set.

c. Toggle-operated POWER circuit breaker CB1, press to test POWER indicator lamp DS1, and TOTAL HOURS meter M1 are on the front of the power control panel. All other operating switches and indicator lamps used to operate the IFF set are on the control box.

4-3. Turning On the IFF Set
(fig. 12–3)

Primary power (+28 vdc) is applied from the associated radar to the IFF set. For the purpose of this discussion of the power distribution system, toggle-operated POWER circuit breaker CB1 on the power control panel and toggle-operated POWER circuit breaker CB1 on the control box are both set to OFF. The radar trigger is present from the associated radar; synchronizer, processor, and receiver-transmitter POWER circuit breakers are set to ON; and a valid code is inserted in the interrogator computer. The IFF set can be safely turned on with any existing combination of switch settings.

a. Momentarily depress press to test POWER lamp DS1 on the power control panel. Lamp DS1 should light indicating that +28 vdc is applied to the IFF set.

b. Setting toggle-operated POWER circuit breaker CB1 on the power control panel to ON applies primary power to the control box.

c. When toggle-operated POWER circuit breaker CB1 on the control box is set to ON, power relay K1 on the power control panel is energized by the power relay enable line (+28 vdc). This results in the following:

(1) POWER lamp DS1 on the power control panel lights and TOTAL HOURS meter M1 starts.

(2) The power lamp enable line (chassis ground) lights POWER indicator lamp DS2 on the control box.

(3) Primary power (+28 vdc) is applied to all assemblies of the IFF set and to the interrogator computer.

(4) One or more of the four red SELF TEST indicator lamps, SYN (DS5), PROC (DS8), KIR (DS6), or R/T (DS9) should light, as indicated below.

NOTE

The remote error indicator (part of the associated radar) should be enabled and remain enabled for the duration of time that any of the SELF TEST indicator lamps are lighted.

(*a*) R/T SELF TEST lamp DS9 normally lights and remains lighted for approximately 60 seconds, the initial receiver-transmitter warm-up delay time. During this period, RF challenge pulses cannot be transmitted. A fault in the receiver-transmitter is indicated if the R/T SELF TEST lamp remains on after the initial 60-second warm-up delay is completed and after momentarily depressing RESET switch on the receiver-transmitter front panel.

(*b*) The other three SELF TEST lamps, SYNC, PROC, and KIR, may or may not light, depending upon initial conditions in their self-test circuits. Within 5 seconds after CB1 on the control box is set to ON, they should all turn off. Such initial fault indications are normal because the respective self-test circuits contain fault storage flip-flops whose initial states are indeterminate when power is first applied. These initial fault indications should automatically be corrected within 5 seconds. If they are not, the corresponding assembly contains an actual fault.

(*c*) If more than one SELF TEST lamp remains lighted after the initial conditions have had a chance to correct themselves, indicating faults in more than one assembly or a fault in one assembly causing faults in others, the PROCESSOR switch should be set to BYPASS and the MODE SELECT switch to any sif mode. Then the assemblies indicated by the lighted lamps should be checked in the following order of preference: synchronizer, receiver-transmitter, processor.

d. PANEL switch S3, depending on its setting at BRIGHT, DIM, or OFF, controls the lighting of the four front panel edge lights DS3, DS4, DS7, and DS10 and also the lamps in CODE SELECT switch assemblies A3 through A12. Lighting of the CODE SELECT switch assembly lamps is enabled by the setting of MODE SELECT switch S6B front.

(1) With MODE SELECT switch S6 set to 1, switch S6B front, contact 2, enables lamps in CODE SELECT switch assemblies A3 and A4. Setting PANEL switch S3 to BRIGHT applies +28 vdc through the lamps in assemblies A3 and A4 as well as through shunt resistor A2R4. Setting PANEL switch S3 to DIM places series resistor A2R5 into the circuit, explained above, which causes the lights to dim.

(2) With MODE SELECT switch S6 set to 2 or 3/A, switch S6B front, contact 3 or 4, respectively, enable lamps in CODE SELECT switch assemblies A5 through A8 or A9 through A12, respectively. Setting PANEL switch S3 to BRIGHT applies +28 vdc directly to the selected lamps. Setting PANEL switch S3 to DIM places series resistor A2R5 into the circuit causing the lights to dim.

e. The light intensity of the POWER, SELF TEST, and CHALLENGE indicator lamps, can be varied by their mechanical shutters. They are turned clockwise to dim them, counterclockwise to brighten them. To vary the intensity of the SELF-TEST indicator lamps and the CHALLENGE lamp, depress LAMP TEST switch S5 as long as is required to make adjustments.

4-4. Confidence Checks

(fig. 12–4)

Two confidence checks are provided by means of LAMP TEST pushbutton switch S5 and the TEST position of spring-loaded CHALLENGE switch S1. These checks can be made at any convenient time during operation, but the first chance occurs immediately after turning on the IFF set, while challenging is prevented during the 60-second warmup period in the receiver-transmitter.

a. LAMP TEST Pushbutton Switch S5. LAMP TEST pushbutton switch S5 is pressed to check the operation of green CHALLENGE lamp DS1 and the four red SELF TEST lamps, DS5 (synchronizer), DS6 (interrogator computer), DS8 (processor), and DS9 (receiver-transmitter). This check

does not interfere with challenging or with any radar scope display, and may therefore be made whenever desired. If it is made during the initial 60-second delay while the receiver-transmitter is warming up, the R/T SELF TEST fault lamp will already be on, and it will remain on for the full 60 seconds.

(1) When pressed, one section of LAMP TEST pushbutton switch S5 connects +28 vdc to lamp driver board 2A1. The +28 volts is applied to the four SELF TEST lamp drive lines through OR gates CR4 through CR7 and to the CHALLENGE lamp drive line through OR gate CR3. In each case, the lamp test voltage is substituted for the output of the corresponding lamp driver transistor, Q7, Q6, Q4, Q3, and Q2, respectively.

(2) The other section of S5 is used to check the operation of relay K1 on the power control panel. If the POWER lamps on the power control panel and control box do not light with both POWER circuit breakers ON, but pressing S5 lights only the control box POWER lamp, relay K1 or its enable line is faulty.

b. CHALLENGE Switch S1. Spring-loaded CHALLENGE switch S1, when held at its TEST position, initiates the testing of the processor for proper processing of decoded friend replies in each of its 47 range boxes. This check, which must be made with the PROCESSOR switch in its IN position, interferes with challenging because it uses the CHALLENGE switch and also fills the radar scope display with test target video. It should only be made when challenging is not required and the test target video in the scope display is not objectionable. Refer to the associated radar technical manual for the detailed procedure required to condition the display to accept test target video.

(1) In operation, the spring-loaded CHALLENGE switch, when held in its TEST position, supplies a self-test enable (test target enable) for the coding system test target generator. This enable, a ground, causes the test target generator to deliver simulated decoded friend replies (test target video) to the reply processing system in the processor. The replies are processed and then fed for display on the radar scope.

(2) The generated test target video produces a pattern that simulates a friend transponder in every one of 47 range boxes with a time separation in a spiral display in which the results of processing can be examined individually for each range box. See TM 11–5895–687–12 for an illustration of a satisfactory display of this type.

4-5. Preparing to Challenge (fig. 12–4)

Preparing to challenge consists of various combinations of switch settings which are dependent on the desired mode of operation (sif modes 1, 2, or 3/A, or mode 4 codes A or B). Paragraphs 4–6 and 4–7 describe the various modes of operation and the functioning of the various switches required for each operation.

4-6. Challenging in the Sif Modes (fig. 12–4)

Challenging in sif modes 1, 2, or 3A is done by setting MODE SELECT S6 to the required mode; CODE SELECT switch assemblies A3 through A12 to the code required for operation in each mode; and, as required, SIF REPLIES switch S7 set to CODED or held to ALL, PROCESSOR switch S4 set to IN or held to BYPASS, and GTC switch S2 set to ON or OFF. With all switches set, challenging occurs when either CHALLENGE switch S1 is held to ON or an external challenge enable is applied from the associated radar.

a. MODE SELECT Switch S6. MODE SELECT switch S6 is a 3–section, 6–position rotary switch. Three positions (1, 2, and 3/A) are used when challenging in the sif modes of operation. The other three positions are used when challenging in mode 4 (para 4–7).

b. CODE SELECT Switch Assemblies A3 through A12. The 10 pushbutton CODE SELECT switch assemblies generate the code digit enable outputs used in the coding system when challenging in the sif modes (1, 2, or 3/A). Two switch assemblies, A3 and A4, are required for mode 1, and four assemblies each, A5 through A8, and A9 through A12, for modes 2 and 3/A, respectively.

(1) The switch assemblies in the selected mode of operation are activated by a corresponding position (1, 2, or 3/A) of MODE SELECT switch S6, which supplies an operating ground to the common (C) terminal of the switch assemblies

used, as well as lighting the selected switch assembly lamps, as explained in paragraph 4–3*d*.

(2) Except for switch assembly A4, each switch assembly has a 3–pole, 8–position rotary switch, an indicating lamp, and three isolating diodes connected to provide three code digit enable lines representing 2^1, 2^2, designated by the numbers 1, 2, and 4. These correspond to their values as a three-bit binary representation (ground = 1) of the numerical switch setting. Thus, these switch assemblies can count from zero to seven. Their readouts, numbered from 0 to 7, advance one unit each time they are pressed, the sequence repeating after 7.

(3) A4 contains a 2–pole, 4–position rotary switch, an indicating lamp, and two isolating diodes connected to provide two code digit enable lines representing 2^0 and 2^1, designated by the numbers 1 and 2. These correspond to their values as a 2–bit binary representation of the numerical switch setting. Thus, this switch assembly can count from zero to three. Its readouts, numbered 0 to 3, advance one unit each time they are pressed, the sequence repeating after 3.

(4) The first digit of each mode is designated A, the second B, the third C, and the fourth D. Thus, the mode 1 reply code consists of only A and B digits, while the modes 2 and 3/A codes consist of A, B, C, and D digits. The table below shows the three-bit binary representation of the numberical switch settings for a typical CODE SELECT switch assembly, A3 in MODE 1, which contains the first, or A digit, of the two digit mode 1 reply code. It supplies the A1, A2, and A4 code digit enables when challenging in mode 1.

Setting of Switch Assy A3	*Code Digit Enable*			*Binary Representation*
	A4(2^2)	*A2(2^1)*	*A1(2^0)*	
0	Open	Open	Open	000
1	Open	Open	Grd	001
2	Open	Grd	Open	010
3	Open	Grd	Grd	011
4	Grd	Open	Open	100
5	Grd	Open	Grd	101
6	Grd	Grd	Open	110
7	Grd	Grd	Grd	111

(5) Figure 12–3 shows the code digit enables generated by each CODE SELECT switch assembly arranged by sif mode of operation.

(6) Operation of the lamps in each switch assembly was described in para 4–3*d*. (All 10 lamps receive a common +28 vdc while MODE SELECT switch S6B–front supplies the ground returns to light the lamps in the mode of operation selected.)

c. SIF REPLIES Switch S7. When challenging is done in an sif mode, the decoding of transponder replies, in the synchronizer, yields two types of decoded reply video: correct code video and bracket decoded video.

(1) Correct code video is produced only by those coded replies, if present, whose coding matches the settings of the corresponding CODE SELECT switch assemblies.

(2) Bracket decoded video is produced by all sif replies, regardless of their coding. It may or may not be included in the processing for use as IFF display video, depending on the position of SIF REPLIES switch S7.

(*a*) Spring-loaded SIF REPLIES switch S7, in its normal CODED position, disables the bracket decode enable line by making it an open circuit. This allows only the correct code video to be processed for use as IFF display video.

(*b*) When spring-loaded SIF REPLIES switch S7 is held at ALL, the bracket decode enable line is a ground, and the bracket decoded video is made available for processing as IFF display video.

d. PROCESSOR Switch S4. PROCESSOR switch S4 supplies the processor bypass enable output to the CHALLENGE lamp logic on lamp driver card 2A1, and through the synchronizer to the reply processing system. When the PROCESSOR switch is in its normal position at IN, the processor bypass enable is an open circuit, allowing the processor to provide processed video to the IFF display. When the PROCESSOR switch is set at BYPASS, the processor bypass enable is a ground, forcing the delivery of unprocessed IFF display video. The processor bypass enable is used only when the processor functions are not usable and must be bypassed (PROC SELF TEST fault indicator DS8 is lighted, and a test target display indicates a malfunctioning processor).

e. GTC Switch S2. GTC switch S2 supplies the gtc enable output to the receiver-transmitter. When

the switch is at ON, the gtc enable is a ground, enabling the gain time control function of the receiver-transmitter; at OFF, the gtc enable is an open circuit, disabling the gain time control function.

f. Mode 1 Challenging. Challenging in mode 1 is done by setting MODE SELECT switch S6 to 1; CODE SELECT switch assemblies A3 and A4 to the required code; and, as required, PROCESSOR switch to IN or BYPASS, and SIF REPLIES switch set to CODED or held to ALL. With all switches set, challenging occurs when either CHALLENGE switch S1 is held to ON or an external challenge enable (ground) is applied from the associated radar.

(1) MODE SELECT switch S6A front, contact 2, provides a mode 1 enable (ground) to CODE SELECT switch assemblies A3 and A4; to lamp driver card A1 which results in the lighting of CHALLENGE lamp DS1; and to circuits within the synchronizer.

(2) MODE SELECT switch S6B front, contact 2, provides a ground for the lamps in CODE SELECT switch assemblies A3 and A4. (Ground lines to all other MODE SELECT switch assemblies are open.)

(3) MODE SELECT switch S6B rear, provides an sif enable (ground) to lamp driver card A1 which stops any kir fault indicator enable from lighting KIR SELF TEST fault indicator lamp DS6.

(4) CODE SELECT switch assemblies A3 and A4, depending on their settings, provide code digit enables A1, A2, A4, B1, and B2 to the synchronizer.

g. Mode 2 Challenging. Challenging in mode 2 is the same as that in mode 1 except that MODE SELECT switch S6 is set to 2 and CODE SELECT switch assemblies A5 through A8 are set to the required code.

(1) MODE SELECT switch S6A front, contact 3, provides a mode 2 enable (ground) to CODE SELECT switch assemblies A5 through A8; and to lamp driver card A1 (as in *e* (1) above).

(2) MODE SELECT switch S6B front, contact 3, provides a ground for the lamps in CODE SELECT switch assemblies A5 through A8.

(3) MODE SELECT switch S6B rear, contact 3, provides an sif enable to lamp driver card A1 (as in *e* (3) above).

(4) CODE SELECT switch assemblies A5 through A8, depending on their settings, provide code digit enables A1 through D4 to the synchronizer.

h. Mode 3/A Challenging. Challenging in mode 3/A is the same as that of mode 2, except that MODE SELECT switch S6 is set to 3/A, and CODE SELECT switch assemblies A9 through A12 are set to the required code.

4-7. Challenging in Mode 4
(fig. 12–4)

Challenging in mode 4 is done by setting MODE SELECT switch S6 to 4; and, as required, MODE 4 switch S8 to A or B, and PROCESSOR switch to IN or BYPASS. When all switches are set, challenging occurs when either CHALLENGE switch S1 is set to ON or an external challenge enable (ground) is applied from the associated radar.

a. MODE SELECT Switch S6. MODE SELECT switch S6 provides 3 positions for use when challenging in mode 4 (4, TEST 4, and LOCKOUT OVERRIDE). TEST 4 and LOCKOUT OVERRIDE positions are guarded. The guard must be pulled out before either of these two positions can be selected. These positions are also spring-loaded which requires that the switch be held in order to maintain the selected position.

(1) When set to 4 (contact 5), TEST 4 (contact 1), or LOCKOUT OVERRIDE (contact 6), switch S6A front, provides a mode 4 enable to the interrogator computer where it serves as a mode 4 challenge control; to the synchronizer coding circuits to initiate mode 4 operation; and to lamp driver card A1 which results in the lighting of CHALLENGE indicator lamp DS1.

(2) When set to TEST 4, switch S6B front, contact 1, applies a mode 4 test enable to the interrogator computer ((*a*) below) and when set to LOCKOUT OVERRIDE switch S6B front, contact 6, applies a mode 4 noise alarm override to the interrogator computer ((b) below).

(*a*) The TEST 4 position of this section supplies a mode 4 test enable ground (verification

bit no. 1) that modifies the challenge encoding in the interrogator computer. Although the resulting challenges appear normal, they are actually test challenges to which friendly mode 4 transponders can reply only as the result of special transponder operator action.

(*b*) The LOCKOUT OVERRIDE position of this section is available to override a low randomness fault condition in the interrogator computer that locks out (inhibits) the video outputs in that unit during mode 4 operation, preventing the transmission of improperly coded challenge words. This lockout condition may also be due to any fault in the self-test circuits, including zeroized code, as indicated by the KIR SELF-TEST lamp being on and the CHALLENGE lamp being off. If the lockout is caused by the low randomness condition, it can be overridden by holding S6 in its LOCKOUT OVERRIDE position. This grounds the mode 4 noise alarm override output to the interrogator computer. The low randomness condition is the only fault that can be overridden to force the interrogator computer to deliver its video outputs even though they are impaired. If the fault is indeed due to this condition, the KIR fault indicator enable line will be normalized (overridden), the KIR SELF TEST lamp will go off and the CHALLENGE lamp will go on; this condition prevails as long as S6 is held in its LOCKOUT OVERRIDE position. If the fault was not due to a low randomness condition, the interrogator computer will not be restored to operation, and there will be no change in the CHALLENGE and KIR SELF TEST lamp indications: the CHALLENGE lamp will remain off, the KIR SELF TEST lamp on.

NOTE

The use of the LOCKOUT OVERRIDE position of S6 when the KIR SELF TEST lamp is on involves a code security risk and requires special authorization.

b. MODE 4 Switch S8. MODE 4 switch S8 is the remote code control switch for mode 4 operation involving the interrogator computer. It has two unguarded positions, A and B, and two guarded momentary positions, CODE HOLD and ZERO, for which a guard must be pulled out before the switch can be held at either position.

NOTE

Do not set this switch to its ZERO position unless specifically required or directed to. To do so will zeroize the mode 4 code.

(1) The code setting inserted in the interrogator computer provides two complete mode 4 codes, Code A and Code B, which can be selected by the two unguarded switch positions, A and B. When MODE 4 switch S8 is set to A, the Code A/B selection output is an open circuit, and Code A is selected; when the switch is set to B, the selection output is a ground, and Code B is selected.

(2) Code security is protected by a combination of mechanical and electrical holds, the loss of any one of which causes the code to be zeroized. The operating requirements involve three external electrical interlocks called zeroize return, refuel hold enable, and landing gear interlock.

(*a*) The zeroize return line is normally a ground (de-energized position of relay K2 on the power control panel).

(*b*) The names of the refuel hold enable and landing gear interlock lines are derived from airborne applications of the interrogator computer. In normal operation, they are open circuits, isolated from each other.

(3) The code, once it is inserted into the interrogator computer and the interrogator computer's access door is closed, is mechanically held in place until +28 vdc primary power is applied to the unit (interrogator computer). This removes the mechanical hold from the code and replaces it with an electrical hold. Thereafter, any loss of power in the interrogator computer for more than about 5 seconds will remove the electrical hold and zeroize the code. To prevent this from occurring when it is necessary to remove power from the interrogator computer for more than 5 seconds, MODE 4 switch S8 must be held in its CODE HOLD position for 15 seconds or more before and during the removal of power and 30 seconds after. This grounds the refuel hold enable and landing gear interlock lines, restores the mechanical hold to the code, and allows electrical power to be removed from the unit.

(4) When the code must be zeroized, the guard on MODE 4 switch S8 is pulled out and the switch is held to ZERO.

4-8. Turning Off the IFF Set
(fig. 12–4)

All power is removed from the IFF set when either toggle-operated POWER circuit breaker CB1 on the control box or toggle-operated POWER circuit breaker CB1 on the power control panel is set to OFF.

NOTE

To protect the code in the interrogator computer from being zeroized by the removal of power for 5 seconds or longer, the guard on MODE 4 switch S8 must be pulled out and the switch held at its CODE HOLD position for at least 15 seconds before and during the removal of power and 30 seconds after.

4-9. Lamp Driver Card 2A1
(fig. 12–4)

Lamp driver card 2A1 contains the circuits for driving the CHALLENGE and SELF TEST lamps and the logic for determining their operating conditions.

4-10. CHALLENGE Lamp DS1
(fig. 12–4)

Green CHALLENGE lamp DS1 is an IFF set confidence indicator.

a. It normally lights whenever the IFF set is generating and transmitting challenges satisfactorily and the IFF set is capable of receiving, decoding, and processing transponder replies, if any. It can indicate satisfactory generation of the essential functions of the IFF set in the presence of specific faults, as indicated by a lighted SELF TEST lamp, under any of the following conditions.

(1) The fault is in the interrogator computer, but an sif challenging mode is selected.

(2) The fault is in the processor, but the PROCESSOR switch has been set to BYPASS.

(3) The fault is in the RF switch of the receiver-transmitter but does not affect the sum channel.

b. If the CHALLENGE lamp does not light while the CHALLENGE switch is held at ON, there is a high probability that transmission is not taking place and that a fault exists in the equipment. However, the generation and transmission of challenges may still take place, and transponder replies may still be received, decoded, and processed, but performance will probably be degraded in one or more of the following ways:

(1) The VSWR (voltage standing wave ratio) in the sum RF path to the associated radar is higher than the maximum allowable.

(2) The transmitted RF challenge pulses are below the minimum acceptable power level.

NOTE

It is not possible for the CHALLENGE lamp and the SYN SELF TEST lamp to be on simultaneously as there is no way to override a synchronizer fault.

4-11. CHALLENGE Lamp Driver
(fig. 12–4)

The CHALLENGE lamp logic controls the CHALLENGE lamp driver circuit, which consists of diodes CR15 and CR8, amplifier Q1, and CHALLENGE lamp driver Q2.

a. Six low inputs to the AND gate consisting of CR15 (one input) and CR8 (five inputs) result in a high output that keeps the CHALLENGE lamp on.

b. On the other hand, a single high input to the same AND gate results in a low output that keeps the CHALLENGE lamp off.

NOTE

The operation of the CHALLENGE lamp depends directly on the operation of the four SELF TEST lamps.

4-12. SELF TEST Lamps
(fig. 12–4)

The four red SELF TEST lamps light to indicate a fault in one of the three IFF assemblies or in the interrogator computer: SYN (DS5, synchronizer), KIR (DS6, interrogator computer), PROC (DS8, processor), and R/T (DS9, receiver-transmitter). The SYN SELF TEST fault lamp lights if a fault is

detected in any module of the synchronizer, if the IFF set is not receiving radar triggers from the associated radar, or if the radar triggers being received are abnormal. The KIR SELF TEST lamp lights if a low randomness condition exists in the mode 4 code, if the interrogator computer detects a fault in its circuitry, or if there is no code set into the interrogator computer. The PROC SELF TEST lamp lights if a fault is detected in any one of the processor modules. The R/T SELF TEST lamp lights during the 60–second warmup period after equipment turn-on, if a fault is detected in any of the receiver-transmitter modules.

4-13. SELF TEST Lamp Drivers
(fig. 12–7)

Each of the four lamp drivers, fed by its fault indicator enable input, operates in the same way.

a. A ground low (fault) input at any of the four fault indicator enable lines will supply an inverted high output from its lamp driver, turning the corresponding SELF TEST lamp on. (This condition holds regardless of the state of the related circuits fed by the lamp driver.)

b. An open circuit high (normal) input at any of the fault indicator enable lines will supply an inverted low output from its lamp driver, keeping the corresponding SELF TEST lamp off.

4-14. The Mode Enable and Challenge Monitor Enable Lines
(fig. 12–4)

One of the six inputs to the challenge lamp driver, and the only one through diode CR15, is the output of the mode enable OR gate (fig. 12–7).

a. When a challenge is not initiated (with CHALLENGE switch S1 or with an external challenge enable input), all four mode enables and the challenge monitor enable are open circuits. The resulting high output from the mode enable OR gate (fig. 12–4), which consists of resistor R17, and diodes CR16 through CR19, is applied to diode CR15. This high causes transistor Q1 to conduct and transistor Q2 to cutoff, keeping CHALLENGE lamp DS1 off.

b. The high output from the mode enable OR gate is also applied to inverter Q8, which turns Q8 on. The resulting low output, uninhibited by the open circuited challenge monitor enable line, is applied through diode CR21 to back bias diode CR8 and CHALLENGE lamp DS1 remains off (fig. 12–3).

c. When a challenge is initiated and transmitted, the selected mode enable line and the challenge monitor enable line are grounds. This results in a low output from the mode enable OR gate to be applied to diode CR15 and to inverter Q8. Diode CR15 is then back biased and cutoff. The challenge monitor ground signal cuts off inverter Q8 and is applied through diode CR21 to diode CR8. The low output from diodes CR8 and CR15 causes amplifier Q1 to cutoff and CHALLENGE lamp driver Q2 to conduct which lights CHALLENGE lamp DS1.

d. If the challenge monitor circuit in the RF system senses that challenges are not being generated or are not being generated satisfactorily (a sum channel fault) it does not ground the challenge monitor enable line, keeping it an open circuit high, and the high output from Q8 is fed through CR21 to CR8, which causes amplifier Q1 to conduct, cutting off amplifier Q2 and turning the CHALLENGE lamp off.

4-15. Synchronizer Fault Indicator Enable Line

a. Synchronizer Normal. During normal operation and when challenging, the synchronizer fault enable line is an open circuit. SYN lamp driver Q3 is not conducting and the resultant low output disables SYN SELF TEST lamp DS5. The low output of SYN lamp driver Q3 provides reverse bias for diodes CR14 and CR8, keeping them cutoff, amplifier Q1 remains cut off, challenge lamp driver Q2 is conducting and CHALLENGE lamp DS1 is on.

b. Synchronizer Fault. When a fault is detected in the synchronizer the synchronizer fault indicator enable line becomes a ground. This low input causes SYN lamp driver Q3 to conduct. The resultant high output lights SYN SELF TEST lamp DS5 and is applied through diodes CR14 and CR8 to turn on amplifier Q1 which cuts off challenge lamp driver Q2 and CHALLENGE lamp DS1 goes off.

4-16. Processor Fault Indicator Enable Line
(fig. 12–7)

a. Processor Normal. During normal operation and when challenging, the processor fault enable line is an open circuit. PROC lamp driver Q6 is not

conducting and the resultant low output disables PROC SELF TEST lamp DS8. This low output provides reverse bias for diodes CR12 and CR8, keeping them cutoff, amplifier Q1 remains cutoff, challenge lamp driver Q2 is conducting and CHALLENGE lamp DS1 is on.

b. Processor Fault; Processor Bypass. When a fault is detected in the processor, the processor fault indicator line becomes a ground. With PROCESSOR switch S4 (fig. 12–4) set to BYPASS, the processor bypass enable line (fig. 12–7) is also a ground. The low processor fault enable input causes PROC lamp driver Q6 to conduct. The resultant high output lights PROC SELF TEST lamp DS8 and is applied through resistor R15 to diode CR11. The low processor bypass enable input causes diode CR11 to conduct, maintaining reverse bias on diodes CR12 and CR8, and amplifier Q1. CHALLENGE lamp driver Q2 remains in conduction and CHALLENGE lamp DS1 remains on.

c. Processor Fault; Processor In. When a fault is detected in the processor and PROCESSOR switch S4 (fig. 12–4) is set to IN, the processor bypass enable line (fig. 12–7) becomes a high. In addition to lighting PROC SELF TEST lamp (*b* above) the high output from PROC lamp driver Q6 is applied through resistor R15 and diodes CR12 and CR8 to amplifier Q1. Amplifier Q1 conducts, CHALLENGE lamp driver Q2 cuts off and CHALLENGE lamp DS1 goes off.

4-17. R/t Fault Indicator Enable Line (fig. 12–7)

a. R/t Normal. During normal operation, and when challenging, the r/t fault indicator enable line is open and the isls pulse inhibit line is a ground. R/t lamp driver Q4 and inverter Q5 are not conducting. The resultant low outputs disable R/T SELF TEST lamp DS9 and provide reverse bias for diodes CR13 and CR8. Amplifier Q1 remains cutoff, CHALLENGE lamp driver Q2 is conducting and CHALLENGE lamp DS1 is on.

b. R/t Fault in RF Switch; Sum Channel Normal. When an RF switch difference channel fault is detected and the sum channel is normal, an isls pulse inhibit is applied to inverter Q5 and to the synchronizer. The synchronizer will cease generation of isls pulses and transmission of interrogations may be resumed. The r/t fault indicator enable line becomes a ground which causes R/t lamp driver Q4 to conduct. The resultant high output of Q4 lights R/T SELF TEST lamp DS9, and is applied through resistor R8 to diode CR13, which would normally provide forward bias to CR13, however, the high isls input to inverter Q5 causes Q5 to conduct, providing a low output which overrides the high output of r/t lamp driver Q4, and diode CR13 remains cutoff. At this time, the R/T SELF TEST lamp is lighted, indicating a receiver-transmitter fault, and CHALLENGE lamp DS1 is lighted, indicating that the receiver-transmitter is challenging.

c. R/t Fault in RF Switch; Sum Channel Fault. When an RF switch sum channel fault is detected, all conditions are the same as in *b* above, except that the challenge monitor enable line becomes an open (high) circuit, permitting inverter Q8 to conduct. The high output from inverter Q8 is applied through diodes CR21 and CR8 to turn on amplifier Q1 which cuts off CHALLENGE lamp driver Q2, and turns off CHALLENGE lamp DS1.

d. R/t Fault — Not in RF Switch. When a fault is detected, other than an RF switch fault, the isls pulse inhibit line remains a ground and r/t fault indicator enable line becomes a ground. The resultant high output of r/t lamp driver Q4 lights the R/T SELF TEST lamp, and is applied through diodes CR13 and CR8 to turn on amplifier Q1 which cuts off CHALLENGE lamp driver Q2, and turns off CHALLENGE lamp DS1.

4-18. Kir Fault Indicator Enable Line (fig. 12–7)

a. Interrogator Computer Normal. During normal operation and when challenging, the kir fault indicator enable line is an open circuit. Kir lamp driver Q7 is not conducting and the resultant low output disables KIR SELF TEST lamp DS6. This low output provides reverse bias to diodes CR10 and CR8, amplifier Q1 is cut off, CHALLENGE lamp driver Q2 is conducting, and CHALLENGE lamp DS1 is on.

b. Interrogator Computer Fault; Sif Operation. When operating in one of the sif modes (modes 1, 2, or 3/A) the sif enable to diode CR9 is a ground. When a fault is detected in the interrogator computer, the kir fault indicator enable becomes a ground which causes kir lamp driver Q7 to conduct. The resultant high output lights KIR

SELF TEST lamp DS6 and is applied through resistor R14 to diodes CR10 and CR9. Diode CR9 conducts and the resultant low output overrides the high at diode CR10. At this time the KIR SELF TEST lamp is on, indicating a fault in the interrogator computer; and CHALLENGE lamp DS1 is on, indicating that challenges are being transmitted.

c. Interrogator Computer Fault; Mode 4 Operation. When operating in mode 4 the sif enable is an open circuit. When a fault is detected in the interrogator computer the kir fault indicator enable becomes a ground which causes kir lamp driver Q7 to conduct. The resultant high output lights KIR SELF TEST lamp DS6 and is applied through diodes CR10 and CR8 to turn on amplifier Q1 which cuts off CHALLENGE lamp driver Q2 and turns off CHALLENGE lamp DS1.

d. Interrogator Computer Fault; Low Randomness Condition. If a low randomness condition exists in the interrogator computer, and if MODE SELECT switch S6 is held at LOCKOUT OVERRIDE, the kir fault indicator enable will become an open through the mode 4 noise alarm override line, the CHALLENGE lamp will go on, and the KIR SELF TEST lamp will go off.

4-19. Remote Error Indicator Card 2A2 (fig. 12–4)

Remote error indicator card provides a remote error indicator enable to the associated radar whenever a fault is detected in the IFF set, or whenever the IFF set is not turned on.

a. No Fault. When no faults are detected in the IFF set, all fault indicator enable inputs to error indicator OR gate CR1 through CR4 are high. Error relay driver Q1 is conducting, error relay K1 is energized, and the remote error indication enable line is an open circuit.

b. Fault. Whenever a fault is detected in the IFF set, the associated fault indicator enable (synchronizer, processor, r/t, or kir) becomes a ground. This low is applied through error indicator OR gate to cutoff error relay driver Q1, which deenergizes error relay K1. Contacts B2 and B1 on relay K1 close to create a closed circuit for the remote error indicator enable line. Error relay K1 is also deenergized when no power is applied to the IFF set.

CHAPTER 5

GENERAL MAINTENANCE INFORMATION

NOTE:

This part of the manual contains information pertinent to direct support, general support, and depot maintenance. The amount of repair that can be performed by units having direct support, general support, and depot responsibility is indicated in the maintenance allocation chart (appendix C, TM 11–5895–678–12).

Section 1. Introduction

5-1. Purpose

a. General. The information contained in this chapter covers general items common to the complete AN/TPX–50 and specifics pertaining to the control box and interrogator group case and is intended to aid the repairman in locating and correcting equipment trouble causing abnormal operation and then checking the serviceability of repaired equipment in a minimum amount of time. Direct support, general support, and depot maintenance instructions for the processor, synchronizer, and receiver-transmitter are contained in TM 11–5895–687–35–2 (processor), TM 11–5895–687–35–3 (synchronizer), and TM 11–5895–687–35–4 (receiver-transmitter). Instructions for performing preventive maintenance and lubrication are contained in the organizational maintenance manual (TM 11–5895–687–12). This information is provided to keep the equipment in good working order so that breakdowns and needless interruptions in operation will be kept to a minimum.

b. Detecting Faulty Operation. Indications of both normal and abnormal operation are provided by means of SELF-TEST and FAULT lamps which are covered in the troubleshooting charts contained in this part of the manual (*c* below). Normal indications that should be obtained on meters, are listed in each troubleshooting and repair chapter.

c. Locating Trouble. The following type troubleshooting charts are provided to aid in locating trouble in a minimum amount of time.

(1) *Troubleshooting based on starting procedure.* A troubleshooting chart based on starting procedure (ch. 6) is designed to enable the repairman to locate trouble based on indications obtained while starting the equipment.

(2) *System symptom troubleshooting charts.* A system symptom troubleshooting chart is located in each system troubleshooting and repair chapter. The charts are based on symptoms which indicate the location of trouble in the system.

(3) *Module troubleshooting charts.* A module troubleshooting chart is located in each module troubleshooting and repair chapter. The charts are based on symptoms which indicate the location of trouble in the module.

(4) *Printed wiring card troubleshooting charts.* Printed wiring card troubleshooting charts are designed to locate trouble on a card when the card is installed in operating equipment (hot mock-up). These charts are located in the printed wiring card troubleshooting and repair chapter.

d. Correcting Trouble. The following information is included to aid in correcting equipment trouble causing faulty operation.

(1) Corrective measures are given in each troubleshooting chart.

(2) Paragraphs covering removal and replacement of parts, where applicable, follow the last troubleshooting procedure in each chapter.

(3) A separate section, where applicable, in each troubleshooting chapter is devoted to the alignment of the system covered by the chapter.

(4) Instructions for performing an overall alignment of the IFF set are contained in chapter 9 of this manual.

(5) Instructions for testing each repaired component of the IFF set are contained in the troubleshooting and repair chapter which pertains to the repaired component.

e. Checking Serviceability. Test procedures designed to check serviceability of the repaired equipment, where applicable, are included in each troubleshooting and repair chapter following the alignment procedure.

5-2. Troubleshooting Techniques

a. General. To be effective, troubleshooting the IFF set must be systematic. It is seldom possible to observe a symptom of trouble and immediately diagnose the cause. Generally, it will be necessary to perform a sequence of operational checks, observations, and measurements before the cause of trouble is revealed. If the proper sequence is followed, the trouble will be traced to an assembly of the IFF set by observing SELF TEST fault indicator lamps, to a module within the assembly by observing FAULT indicator lamps and, by using test procedures, to a printed wiring card within the module, and finally to a component or part. The sequence of steps is referred to commonly as sectionalization, localization, and isolation.

b. Sectionalization. The first aim in troubleshooting is to sectionalize the trouble an assembly or a module of the IFF set. Sectionalization to an assembly can be accomplished through observation of SELF TEST lamps, and to a module, by observation of the FAULT lamps on the assembly.

c. Localization. After the trouble has been sectionalized, the troubleshooting chart based on starting procedure will reference either an appropriate troubleshooting chart for the control box or interrogator group case or the TM for a faulty assembly.

d. Isolation. After the trouble has been localized to either a system, assembly or module, use visual inspection, waveform analysis, and voltage and resistance measurements to determine the defective part. Transistor test set TS–1836A/U will be of particular help in checking suspected transistors. Both in-circuit and out-of-circuit measurements of Beta may be performed using the TS–1836A/U. Paragraph 5–21 lists typical out-of-circuit Beta and leakage current (I_{CBO}) measurements of transistors typical of those used in the IFF set.

5-3. Troubleshooting Data

a. General. In addition to the troubleshooting charts, other troubleshooting data are supplied to help the repairman rapidly locate the trouble. A list of the specific troubleshooting data, which will help to locate troubles, is given in the *Reference data* paragraph contained in the first section of each troubleshooting chapter. The following types of troubleshooting data are provided to assist the repairman to isolate faulty assemblies, modules and cards.

b. Block Diagrams. The block diagrams give the electrical and mechanical interrelationships among the units, assemblies, modules, and printed-wiring cards of the IFF set. By observing the symptoms and reasoning possible causes, it is often possible to trace the cause of faulty operation to a trouble in a particular block.

c. Cabling Diagram. This diagram and cable list which is located in TM 11–5895–687–12 shows cabling between the units of the IFF set. This type of data can be used to check cabling.

d. Interconnection Diagram. This diagram, (fig. 12–2) shows all of the interconnections between units and assemblies of the IFF set. This data is especially useful for tracing trouble between assemblies.

e. Complete Schematic Diagrams. A complete schematic diagram is provided for each assembly, each module of each of the assemblies, and each card of each of the modules. This type of diagram shows all of the circuitry in the assembly module or card and can be used to aid in determining the faulty part in an assembly.

f. Voltage and Resistance Charts. A voltage and resistance chart is provided for each assembly,

module and card. This type of data provides normal voltage and resistance measurements at all key test points and etched connector pins and is helpful when making voltage and/or resistance measurements to trace the fault to a specific circuit. When using these charts, carefully read the notes and duplicate exactly the conditions under which the readings were obtained (para 5–5).

g. Waveform Illustrations. Waveform illustrations, which are located in the applicable troubleshooting chapters show normal waveforms at significant points and are helpful in locating trouble.

5–4. Waveform Analysis

Waveforms may be observed at various test jacks and at other significant points in the circuits of Interrogator Set AN/TPX–50 by using Oscilloscope AN/USM–281A. Detailed instructions for operating the Oscilloscope are contained in TM 11–6625–1703–15. The normal waveforms that should be obtained at test jacks and other significant points are shown on the waveform illustrations located in each troubleshooting chapter. By comparing observed waveforms with normal waveforms, trouble can sometimes be located quickly.

5–5. Voltage and Resistance Measurements

a. General. Voltage and resistance measurements are an aid in determining circuit conditions and in evaluating significant indications in the course of troubleshooting. Carefully read the notes on the voltage and resistance charts and duplicate exactly the conditions under which the measurements were obtained.

b. Measurement Conditions. Voltage and resistance measurements are to be made with Multimeter AN/PSM–6B. (20,000 ohms per volt). Resistance measurements are to be made on repaired cards, before installation, to insure that no shorts were created during repair. Voltage measurements are to be obtained with the equipment in an operating (hot mockup) situation. All voltage and resistance readings are to be taken with respect to ground.

5–6. AN/TPX–50 Diode Resistances

The following chart lists the out-of-circuit resistances, both in the forward and reverse directions, of semiconductor diodes, voltage rectifiers, and unijunction transistors used in the IFF set. These measurements were made with Multimeter AN/PSM–6B using the resistance scale as listed on the chart. All readings are actual records of measurements on diodes, rectifiers, and unijunction transistors, typical of those used in the IFF set.

Type	Forward resistance in ohms	Meter range setting	Forward resistance in ohms	Meter range setting
		DIODES		
HPA8606	17	RX1	5M	RX10,000
LVA56A	14	RX1	350K	RX10,000
UTR6410R	10	RX1	5M	RX10,000
UTX215	11	RX1	5M	RX10,000
UZ718	13	RX1	5M	RX10,000
UZ720	13	RX1	5M	RX10,000
UZ722	13	RX1	5M	RX10,000
UZ733	15	RX1	5M	RX10,000
UZ5120	14	RX1	5M	RX10,000
UZ5130	15	RX1	5M	RX10,000
UZ5220	13	RX1	5M	RX10,000
UZ5722	12	RX1	5M	RX10,000
1N21G	15	RX1	70K	RX10,000
1N645	15	RX1	5M	RX10,000
1N746A	13	RX1	40K	RX10,000
1N748A	15	RX1	50K	RX10,000
1N750A	14	RX1	70K	RX10,000
1N751A	15	RX1	100K	RX10,000
1N752A	15	RX1	300K	RX10,000
1N753A	15	RX1	300K	RX10,000
1N754A	14	RX1	500K	RX10,000
1N756A	15	RX1	3M	RX10,000
1N829A	100K	RX10,000	300K	RX10,000
1N830A	UNABLE TO TEST			
1N914	20	RX1	5M	RX10,000
1N963B	14	RX1	5M	RX10,000
1N964B	16	RX1	5M	RX10,000
1N965B	17	RX1	5M	RX10,000
1N967B	13	RX1	5M	RX10,000
1N973B	14	RX1	5M	RX10,000
1N1616	12	RX1	5M	RX10,000
1N2991B	12	RX1	5M	RX10,000
1N3023	12	RX1	5M	RX10,000
1N3033B	12	RX1	5M	RX10,000
1N3064	14	RX1	5M	RX10,000
1N3070	17	RX1	5M	RX10,000
1N3613B	11	RX1	5M	RX10,000
1N3885	8	RX1	5M	RX10,000
1N3889R	8	RX1	3M	RX10,000
1N3997RA	12	RX1	160K	RX10,000
1N4454	14	RX1	5M	RX10,000
1N4555B	11	RX1	220K	RX10,000
1N4555RB	11	RX1	500K	RX10,000
1N4719	11	RX1	5M	RX10,000

Type	Forward resistance in ohms	Meter range setting	Backward resistance in ohms	Meter range setting
RECTIFIERS				
SBR–02	Arbitrary pin numbers assigned in a clockwise direction with pin number 1 at the red dot.			
1–2	5M	RX10,000	80K	RX10,000
1–3	5M	RX10,000	250K	RX10,000
1–4	5M	RX10,000	80K	RX10,000
2–3	5M	RX10,000	80K	RX10,000
4–2	5M	RX10,000	5M	RX10,000
4–3	5M	RX10,000	80K	RX10,000
MDA–920–6	Arbitrary pin numbers assigned in a clockwise direction with pin number 1 at +			
2–1	13	RX1	5M	RX10,000
2–4	5M	RX10,000	13	RX1
3–1	13	RX1	5M	RX10,000
3–2	5M	RX10,000	5M	RX10,000
3–4	5M	RX10,000	13	RX1
4–1	90	RX1	5M	RX10,000
MDA–920–6	Pin number assigned as for MWA–920–6			
2–1	13	RX1	5M	RX10,000
2–4	5M	RX10,000	13	RX1
3–1	13	RX1	5M	RX10,000
3–2	5M	RX10,000	5M	RX10,000
3–4	5M	RX10,000	13	RX1
4–1	80	RX1	5M	RX10,000
VR100X/S	Arbitrary pin numbers assigned in a clockwise direction with pin number 1 at the red dot or number 3 at the black dot			
1–2	5M	RX10,000	10	RX1
1–3	5M	RX10,000	35	RX1
1–4	5M	RX10,000	10	RX1
2–3	5M	RX10,000	10	RX1
2–4	5M	RX10,000	5M	RX10,000
3–4	10	RX1	5M	RX10,000
UNIJUNCTION TRANSISTORS				
2N491A				
Emitter–B1	22	RX1	5M	RX10,000
Emitter–B2	45	RX1	5M	RX10,000
2N1772A				
Gate-Cathode	24	RX1	100	RX1
Anode-Cathode	5M	RX10,000	5M	RX10,000
2N1774A				
Gate-Cathode	15	RX1	90	RX1
Anode-Cathode	5M	RX10,000	5M	RX10,000
2N2840				
Emitter–B1	100	RX1	5M	RX10,000
Emitter–B2	80	RX1	5M	RX10,000

5–7. Control, Interrogator Set C–7651/TPX–50 Resistances

The following chart lists the resistances, both forward and reverse directions, of all pins on connector 2J1 on the control box. These measurements were made with Multimeter AN/PSM–6B using the resistance scale as listed on the chart.

	Resistance in ohms			
Pin No.	Meter range	Forward	Meter range	Reverse
A	RX1000	85K	RX1000	INF
B	RX1000	85K	RX1000	INF
C	RX1000	90K	RX1000	INF
D	RX1000	85K	RX1000	INF
E	RX1000	0	RX1000	INF
F	RX1000	INF	RX1000	INF
G	RX1000	INF	RX1000	INF
H	RX1000	INF	RX1000	INF
J	RX1000	INF	RX1000	INF
K	RX1000	INF	RX1000	INF
L	RX1000	INF	RX1000	INF
M	RX1000	INF	RX1000	INF
N	RX1000	INF	RX1000	INF
P	RX1000	INF	RX1000	INF
R	RX1000	INF	RX1000	INF
S	RX1000	INF	RX1000	INF
T	RX1000	INF	RX1000	INF
U	RX1000	INF	RX1000	INF
V	RX1000	INF	RX1000	90K
W	RX1000	50K	RX1000	50K
X	RX1000	85K	RX1000	INF
Y	RX1000	INF	RX1000	INF
Z	RX1000	INF	RX1000	INF
a	RX1000	45K	RX1000	INF
b	RX1000	INF	RX1000	INF
c	RX1000	INF	RX1000	INF
d	RX1000	INF	RX1000	INF
e	RX1000	INF	RX1000	INF
f	RX1000	INF	RX1000	INF
g	RX1000	INF	RX1000	INF
h	RX1000	40K	RX1000	75K
i	RX1000	INF	RX1000	INF
j	RX1000	40K	RX1000	75K
k	RX1000	40K	RX1000	75K
m	RX1000	INF	RX1000	INF
n	RX1000	INF	RX1000	INF
p	RX1000	40K	RX1000	75K
q	RX1000	40K	RX1000	53K
r	RX1000	75K	RX1000	40K
s	RX1000	INF	RX1000	90K
t	RX1000	INF	RX1000	INF
u	RX1000	INF	RX1000	INF
v	RX1000	INF	RX1000	INF
w	RX1000	INF	RX1000	INF
x	RX1000	INF	RX1000	INF
y	RX1000	INF	RX1000	INF
z	RX1000	INF	RX1000	INF
AA	RX1000	INF	RX1000	INF
BB	RX1000	INF	RX1000	75K
CC	RX1000	INF	RX1000	53K
DD	RX1000	50K	RX1000	50K
EE	RX1000	INF	RX1000	INF
FF	RX1	O	RX1	O
GG	RX1000	INF	RX1000	INF
HH	RX1000	INF	RX1000	INF

5-8. Cabinet, Interrogator Set Group CY-6442/TPX-50 Resistances

The following chart lists the resistances, both forward and reverse, of all pins on all connectors of the interrogator group case. These measurements were made with Multimeter AN/PSM–6B, using the resistance scale as listed on the chart, with all assemblies installed in the interrogator group case and with all external cables removed.

	Resistance in ohms			
Pin No.	Meter range	Forward	Meter range	Reverse
J1	RX1	35	RX1	7
J2	RX100	10K	RX100	2.5K
J3	RX100	10K	RX100	50K
J4–A	RX100	10K	RX100	4.3K
J4–B	RX1	100	RX1	95
J4–C	RX100	10K	RX100	4.8K
J4–D	RX10000	1NF	RX10000	INF
J4–E	RX1	34	RX1	83
J4–F	RX1	33	RX1	83
J5–A	RX100	5.7K	RX100	5K
J5–B	RX100	5.9K	RX100	5K
J5–C	RX100	5.9K	RX100	5K
J5–D	RX100	5.7K	RX100	5K
J5–E	RX10	300	RX100	6K
J5–F	RX10000	INF	RX10000	INF
J5–G	RX10000	INF	RX10000	INF
J5–H	RX100	5.9K	RX100	5K
J5–J	RX100	5.9K	RX100	5K
J5–K	RX100	5.9K	RX100	5K
J5–L	RX100	5.9K	RX100	5K
J5–M	RX100	5.9K	RX100	5K
J5–N	RX100	5.9K	RX100	5K
J5–P	RX100	5.9K	RX100	5K
J5–5	RX100	5.9K	RX100	5K
J5–T	RX100	5.9K	RX100	5K
J5–U	RX100	5.9K	RX100	5K
J5–V	RX10000	INF	RX10000	INF
J5–W	RX10000	INF	RX10000	INF
J5–X	RX10000	INF	RX10000	INF
J5–a	RX100	5.7K	RX100	5K
J5–b	RX10000	INF	RX1000	INF
J5–c	RX10000	INF	RX1000	INF
J5–d	RX100	5.7K	RX100	5K
J5–f	RX10000	INF	RX10000	INF
J5–g	RX10	390	RX10	270
J5–h	RX1	4	RX1	0
J5–j	RX1	4	RX1	0
J5–k	RX1	4	RX1	0
J5–m	RX100	6K	RX100	5K
J5–n	RX100	6K	RX100	5K
J5–p	RX10000	INF	RX10000	INF
J5–q	RX10000	INF	RX10000	INF
J5–r	RX1	4	RX1	0
J5–s	RX10	210	RX10	320
J5–t	RX100	6K	RX100	5.2K
J5–DD	RX10000	INF	RX10000	INF
J5–EE	RX1	4	RX1	3
J5–FF	RX1	4	RX1	3
J5–HH	RX10000	INF	RX10000	INF
J6–A	RX10000	INF	RX10000	INF
J6–B	RX10000	INF	RX10000	INF
J6–C	RX10000	INF	RX10000	INF
J6–D	RX1	0	RX1	0
J6–E	RX10000	INF	RX10000	INF
J6–F	RX1000	INF	RX10000	INF
J6–G	RX10000	INF	RX10000	INF
J6–H	RX100	5.7K	RX100	5K
J6–R	RX1	0	RX1	0
J6–U	RX1	0	RX1	0
J6–V	RX1	0	RX1	0
J7–A	RX10000	INF	RX10000	INF
J7–C	RX1	0	RX1	0
J8–A	RX10000	INF	RX10000	INF
J8–B	RX10000	INF	RX10000	INF
J8–C	RX1	0	RX1	0
J8–E	RX10000	INF	RX10000	INF
J9	RX10000	INF	RX10000	INF
J10	RX10000	INF	RX10000	INF

5-9. Reference Designation Number Location Chart

a. To aid in parts location, reference designations have been assigned throughout the IFF set in accordance with the unit numbering method outlined in ASA 432.16–1965 *American Standard Electrical and Electronics Reference Designations.* This method identifies the interrogator group case as the first free-standing enclosure (unit 1), the control box as the second free-standing enclosure (unit 2) and the interrogator computer as the third free-standing inclosure (unit 3). The following chart lists the unit and assembly designations assigned to each major assembly.

Reference	*Common Name*	*Nomenclature*
Unit 1	Interrogator Group	Cabinet, Interrogator Set Group CY–6442/TPX–50
1A1	Processor	Signal Processor CP–936/TPX–50
1A2	Synchronizer	Synchronizer Electrical SN–421/TPX–50
1A3	Receiver-Transmitter	Receiver-Transmitter Radio RT–903/TPX–50.
Unit 2	Control box	Control, Interrogator Set C–7651/TPX–50.

Reference	*Common Name*	*Nomenclature*
2A1	Lamp driver card	
2A2	Remote Error Indicator card	
Unit 3	Interrogator computer	Interrogator Computer KIR–1A/TSEC equipped with Power Supply ZACB/TSEC (28 volts dc).
Subassemblies for Unit 3		Refer to KAM–223/TSEC maintenance manual for KIR–1A/TSEC.

b. The subassemblies and piece parts are similarly identified, each with a class letter and location number, and these are added to the major assembly designation. An example of a complete reference designation for a piece part is 1A1A2A3R1 which identifies the first resistor (R1) on the third card (A3 friend arithmetic card) of the second module (A2, friend arithmetic module) of the first assembly (A1, processor) of the first unit (1, interrogator group).

5-10. Parts Location

a. General. This manual provides illustrations of all parts of the IFF set to assist the repairman during troubleshooting and repairing procedures. Illustrations of organizational maintenance parts located in the control box, and assemblies and modules in the interrogator group case are in TM 11–5895–687–12. Illustrations of card mounted parts are in the form of line drawings usually located on the aprons of the card schematic diagrams. Illustrations of parts mounted in the interrogator group case and within the control box are contained in this portion of the manual.

b. Replacement Parts. When ordering replacement parts ensure that the complete and correct reference designations are used.

5-11. Replacing Modules

a. Removing and Replacing Modules. When removing and replacing modules observe cautions and procedures outlined in TM 11–5895–687–12, paragraphs 5–16 and 5–17.

b. Module Substitution. Do not substitute modules indiscriminately. Substitute a module only when the corresponding FAULT indicator lamp for the module is lit. If a replacement module does not clear the fault, replace the original module into the assembly and refer to the appropriate troubleshooting chart.

5-12. Replacing Printed Wiring Cards

CAUTION

Be sure that power is off when removing or replacing printed wiring cards, in modules which are in installed assemblies.

Removal of printed wiring cards (cards) (*a* below) from a module is accomplished using Printed-Wiring card extractors (extractor) MP1 and MP2, which are contained in Test Facility Set AN/TPM–24(V)3. The MP1 extractor is used to remove cards from the receiver module in the receiver-transmitter. The MP2 extractor is used to remove cards from synchronizer, and processor modules, and from the power supply module of the receiver-transmitter.

a. Removal of Cards. To remove cards from modules proceed as follows:

(1) Slide the appropriate assembly out of the group case (para 5–15, TM 11–5895–687–12) until outgoing slide limit locks engage.

(2) Loosen the two captive screws (fig. 2–5, TM 11–5895–687–12) and raise the card hold-down cover.

(3) Place the hooked ends of the appropriate card extractor through the holes located near the top of each side of the card. Using a firm even pull, remove the card from its connector.

b. Replacement of Cards. Before installing a card ((4) below) in a module observe the precautions in (1) through (3) below.

(1) If the card has been repaired, make resistance measurements to insure that the repair of the card did not create a short circuit.

(2) Clean the etched connector pins of the card using either inhibisol cleaning solvent or a solution of 70 percent alcohol and 30 percent distilled water.

(3) Insure that the mating connector is free from dirt or obstructions.

(4) Install card into its mating connector, observing the guide key, and press firmly into place.

c. Card Substitution. Do not substitute printed wiring cards indiscriminately. Card substitution should be used only when a module is defective (module FAULT indicator lamp is lit) and normal troubleshooting techniques do not localize the trouble to a card. When substituting cards as a troubleshooting aid, proceed as follows:

(1) Remove all cards in question.

(2) Substitute cards that are known to be operable.

(3) If the fault still exists, module FAULT indicator lamp remains lit, replace the original cards and refer to the troubleshooting chart.

(4) If the fault no longer exists, module FAULT indicator lamp is not lit, clean original card connector pins using inhibisol cleaning solvent or solution of 70 percent alcohol and 30 percent distilled water. Replace the original cards one at a time until the fault reappears, then remove the card that caused the fault to reappear, replacing it with a new card.

(5) Continue to replace the cleaned original cards until only the faulty card has actually been replaced.

5-13. Replacing Integrated Circuits

When replacing integrated circuits, use extreme care. Excessive heat can ruin the internal circuit as well as the printed wiring pattern, excessive pulling or bending can break off the terminal leads, and bad connections can result in the shorting or opening of leads. The tools and materials required for this operation include a low power (37.5 watts maximum) soldering iron, a scribe (made of an untinnable metal), non-corrosive flux, and fine (1/32 inch) wire solder. To remove and replace the damaged integrated circuit, perform the operations described below.

a. Apply noncorrosive flux to the area to be worked.

b. Hold the hot tip of the soldering iron against the integrated circuit lead until the solder melts.

c. Using the scribe, gently lift the lead until it is free from the solder point.

d. Proceed to the next integrated circuit lead and repeat steps *a* and *b* above until all leads of the integrated circuit have been removed.

e. When cool, lift the whole integrated circuit from the card.

f. Before installing the replacement integrated circuit, clean the areas to be soldered with cleaning solvent and add noncorrosive flux.

g. Carefully position the replacement integrated circuit on the card with leads aligned to the corresponding printed circuit solder points.

h. Using the scribe, hold the integrated circuit lead in position on the solder joint.

i. Apply the tip of the hot soldering iron to the integrated circuit lead at the solder joint until the lead melts into the solder in solder joint.

j. When solder joint has cooled, remove the scribe.

k. Repeat steps *h* through *j* above for each integrated circuit lead. Care must be taken to prevent solder from short circuiting any of the integrated circuit leads to the case or to each other.

l. Clean board to remove flux and replace conformal coating (para 5–18).

5-14. Replacing Piece Parts

Careless replacement of parts often creates new troubles. When replacing parts, other than integrated circuits, observe the following precautions:

a. Before a part is unsoldered, note the position of the leads. If a part, such as a line filter, a transformer, or a switch, has a number of connections, tag each of the leads in order to make the proper connections when replacing the part. Be careful not to damage other leads by pulling or pushing them away.

b. Make well-soldered joints. A carelessly soldered joint may create a new trouble and is one of the most difficult troubles to locate. Be careful not to allow drops of solder to fall into the equipment as this may cause short circuits.

c. When replacing a part in an RF circuit, place the part in exactly the same position as the original part. A part that has the same electrical value but different physical size may cause trouble in high frequency circuits. In such circuits, use the same type capacitor for replacement and the same lead length because of the self-resonant frequencies which may vary between different types of capacitors. When replacing parts in high frequency circuits, give particular attention to proper grounding, using the same ground as in the original wiring. Failure to observe these precautions when replacing parts in high frequency circuits may result in decreased gain or possibly in unwanted oscillations.

d. Whenever a part has been replaced, make any necessary adjustments and check the performance of the equipment to be sure that the original trouble has been remedied and that no new trouble has developed in the equipment as a result of the repair.

e. In those circuits of the IFF set which are transistorized, use a pencil-type soldering iron with a 25-watt maximum capacity. If the iron must be used with ac, use an isolating transformer between the iron and the line. Do not use a soldering gun; damaging voltages can be induced in circuit components.

f. When soldering transistor leads, solder quickly; whenever wiring permits use a heat sink (such as long-nosed pliers) between the soldered joint and the transistor. Do not clip the leads of replacement transistors; keep the leads as long as possible.

g. Interconnecting wiring in a module is connected to the card connector using contacts which are crimped to the interconnecting harness before the contact is inserted into the rear of the connector. This contact must be removed to replace a broken wire.

5-15. Parts Substitution

a. When substituting parts as a troubleshooting aid, do not substitute circuit elements indiscriminately. Substitute only when all of the following conditions are satisfied:

(1) The trouble has been isolated to a specific stage or integrated circuit.

(2) All other means of locating the defective component have failed.

b. Types of troubles which would satisfy all of the above conditions are: open bypass or coupling capacitors, capacitors that have changed values, an interstage transformer with shorted turns, a defective transistor, and a defective integrated circuit.

c. When an open capacitor is suspected, connect a known good capacitor of equal electrical value across the open capacitor and check the operation of the printed wiring card.

d. When all other possibilities of trouble are ruled out, substitute a good part for the one which is suspected of being defective.

5-16. Cable Check and Repair

a. Shorts. To check a multiconductor cable for shorts between conductors, proceed as follows:

(1) Connect one ohmmeter lead to each cable conductor, one at a time, while performing the following step for each connection.

(2) Connect the second ohmmeter lead to every other conductor in the cable (one conductor at a time).

(3) If the meter indicates zero, a short exists between the two conductors being measured.

(4) If the meter indicates less than infinite but more than zero, the two conductors have a dc leakage path between them.

(5) If the meter indicates infinite, the two conductors are not shorted in any way.

b. Continuity. When checking for continuity, the ohmmeter leads may not be long enough to be connected to both ends of the cable. The following procedure is given as a convenient method of determining the condition of a cable:

(1) Connect a resistor of known value, 50,000 ohms or more, between one end of the suspected cable conductor and ground.

(2) Connect the ohmmeter leads between the conductor and ground at the other end of the cable.

(3) If the meter indicates approximately 50,000 ohms, the conductor has continuity.

(4) If the meter indicates infinite resistance, the conductor is open.

(5) If the meter indicates zero resistance, the conductor is shorted to ground.

(6) If the meter indicates much less than 50,000 ohms, but not necessarily zero, the conductor has a dc leakage path to ground.

c. Repair. Damaged pins in a connector may be replaced. A damaged cable connector cannot be repaired; it must be replaced. Splicing of broken cables is accomplished by placing a male connector on one end and a female connector on the other end. The cables are then joined by mating the two connectors. The procedure for replacing pins and for attaching connectors to cable ends is in paragraph 5–17.

5-17. Repair of Cables W1 and W2 (fig. 5–1)

Repair of cables W1 and W2 consists of removal and replacement of damaged pins and damaged connectors. Cables W1 and W2 are described in *a* and *b* below and repair procedures are described in *c* below. Tools required are listed in paragraph 5–22.

a. Description of Cable W1. Cable W1 is a multiconductor cable having 41 conductors and two connectors. All conductors are AWG20, white insulated, solid wire with the exception of those wires connected to pins FF and EE which are AWG20, black insulated, 19 strand wire and the wire connected to pin HH which is AWG20, red insulated, 19 strand wire. W1P1 is a MS3125F–22–55P connector containing 55 MS3192–A20A pins. W1P2 is a MS3126F–22–55S connector containing 55 MS3192–A20A sockets. All conductors originating at pins on W1P1 are terminated at the same socket designation on W1P2, *for example:* "the wire originating at pin FF on connector W1P1 terminates at socket FF on connector W1P2." Connectors W1P1 and W1P2 and the cable sleeving near the connectors are covered with a boot which is held in place with an epoxy resin.

b. Description of Cable W2. Cable W2 is a multiconnector, wye type cable having 18 conductors and 3 connectors. All conductors originate at connector W2P1 and terminate at either connector W2P2 or W2P3. Connector W2P1 is an amphenol connector, part No. 94–621, containing 6 amphenol sockets, part No. 94–658–08, all of which are used; 25 MS3193A–20A sockets, of which 12 are used; and 4 MS3193–16A sockets, of which 2 are used. W2P3 is a MS3126F–14–19P connector containing 19 MS3192–A20A pins of which 14 are used. W2P2 is a PTO6SE–22–78P connector containing 7 Bendix 21–33012–24 pins of which 6 are used. Connectors W2P2 and W2P3 and the cable sleeving near the connectors are covered with a boot which is held in place with a two part epoxy resin. The following char lists the origin and destination of each of the conductors in cable W.2.

FROM CONNECTOR–	PIN	TO CONNECTOR–	PIN
P1	*1	P2	D
P1	*3	P2	E
P1	*4	P2	C
P1	*6	P2	B
P1	*7	P2	A
P1	*8	P2	F
P1	9	P3	C
P1	12	P1	13
P1	14	P3	A
P1	19	P3	B
P1	**20	P3	R
P1	23	P3	G
P1	**24	P3	S
P1	26	P3	H
P1	***31	P3	V
P1	32	P3	E
P1	33	P3	D
P1	**34	P3	U
P1	37	P3	F

*These conductors are RG–180 cable, the external conductors are connected through the connector shielding to chassis ground within the assemblies to which they connect.

**These conductors are AWG 20, black insulated 19 strand wire.

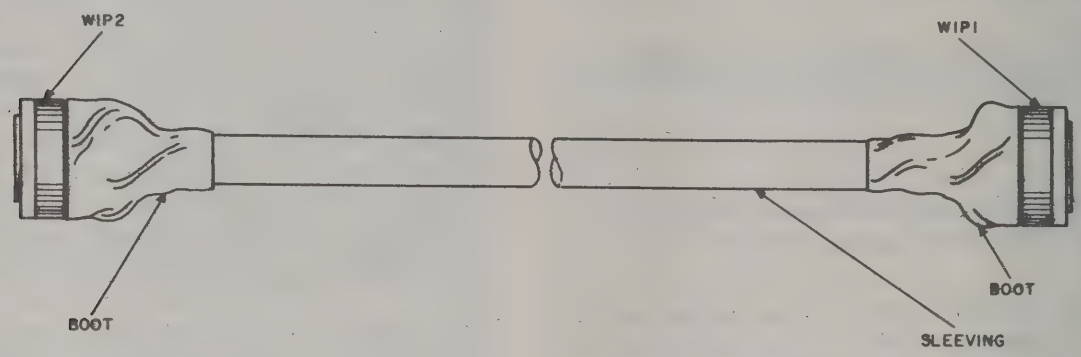
***This conductor is AWG 20, red insulated 19 strand wire. All others are AWG20 white insulated solid wire.

c. Cable Repair Procedures. To replace damaged pins or damaged connectors, refer to figure 5–1 and proceed as follows:

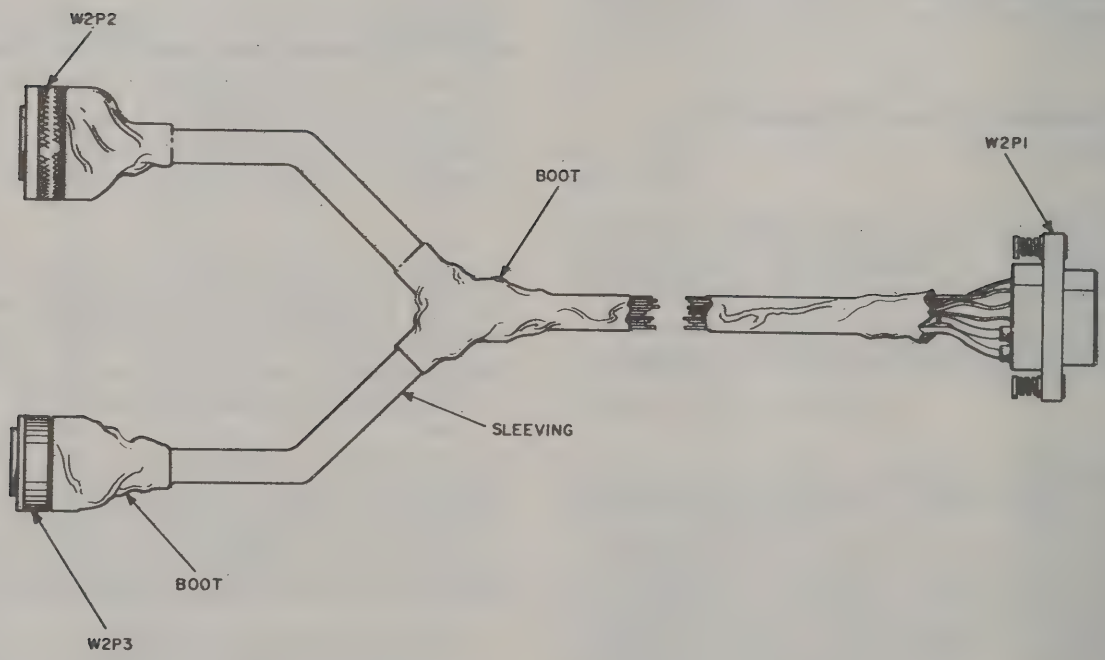
(1) Remove the boot from the connector and from the cable sleeving, by carefully cutting the boot with a sharp knife or razor, taking care not to cut the sleeving or the cable conductors, and peeling the boot away.

NOTE

If a connector is to be replaced, all pins or sockets must be removed. If a pin or socket is to be replaced and no spare pins or sockets are available, remove an unused pin or socket from the connector to replace the damaged one.



CABLE W1



CABLE W2

Figure 5–1. Cables W1 and W2.

CAUTION

Tag all wires being removed with pin designation to expedite replacement and to prevent installation in the wrong positions.

(2) Remove the pin(s) or socket(s) from the connector using the appropriate extracting tool(s) for type of pin to be removed.

(3) Remove damaged pin(s) or socket(s) from the wire by cutting the wire as close to the pin as possible.

(4) Remove 3/16 inch of insulation from the wire. Install new pin or socket wire and crimp, using the appropriate crimping tool.

(5) Insert the pin(s) or socket(s) into the connector using the appropriate insertion tool(s).

(6) Clean the connector and sleeving using No. 320 emery cloth. This will remove all of the epoxy and at the same time will abrade the connector and the cable sleeving.

(7) Abrade the inside of the boot with No. 320 emery cloth.

(8) Remove any emery cloth residue with cleaning solvent.

(9) Prime all areas to be bonded with an adhesive primer. Allow primer to dry for 30 minutes.

(10) Install boot over the connector onto the cable.

(11) Apply epoxy to the inner surface of the boot.

(12) Place the connector pin end on a flat surface and place the boot into position on the upper portion of the connector, ensuring that the boot does not interfere with the retaining ring of the connector. Care must also be taken that no epoxy gets on or under the connector retaining ring.

(13) While holding the boot firmly in place on the connector, apply uniform heat with a heat gun around the boot to shrink the boot onto the connector. During the shrinking, the boot has a tendency to slip off the connector, therefore it must be held firmly until it is completely seated on the connector.

(14) Allow the boot and connector to cool.

(15) Hold the boot in place on the cable sleeving, shrink the boot onto the cable, as in (13) above, until the boot is firmly seated on the sleeving.

(16) Curing times and temperatures for the epoxy are as follows:

(*a*) 45 minutes at 250°F

(*b*) 60 minutes at 200°F

(*c*) 3 hours at 180°

(*d*) 24 hours at room temperature (set to handle)

(*e*) 96 hours at room temperature (cured)

5-18. Repair of Coaxial Cable RG-180 (fig. 5–2)

The following procedures describe the procedures for the repair of coaxial cable RG–180 in cable W2P1 (*a* below) and W2P2 (*b* below).

a. Cable W2P1 Coaxial Cable RG–180 Repair (A, fig. 5–2).

(1) Use extractor tool (AMP part No. 294–238) to remove socket (AMO part No. 94–658–08) from connector W2P1.

(2) Cut coaxial cable RG–180 as close to the socket as possible, insuring that the cut is square.

(3) Slide the boot for the new socket over the coaxial able, ensuring that the ridge of the boot is toward the end of the cable.

(4) Slide the ferrule over the coaxial cable.

(5) Strip 0.575 inch outer insulation from the coaxial cable to expose the double braided outer conductor.

(6) Cut the double braided outer conductor 0.35 inch from the end of the cable.

(7) Flair the double braided outer conductor very slightly, enough to pass over the tip of the body of the socket.

(8) Trim the teflon insulation 0.20 inch from the end of the cable to expose the inner conductor.

(9) Tin the inner conductor and the inside of the base of the pin, and, while maintaining heat on pin, insert inner conductor into pin and allow to cool.

(10) Insert pin into the tip of the body of the socket until a slight click is heard, while ensuring that the double braided outer conductor fits around the outside of the tip of the body of the socket. A slight tug on the cable will insure that the pin is correctly seated.

(11) Slide the ferrule over the double braided outer conductor and use crimping tool (Thomas and Betts part No. WT403) to crimp ferrule.

(12) Slide the boot on the cable to the point where it is flush against the ferrule.

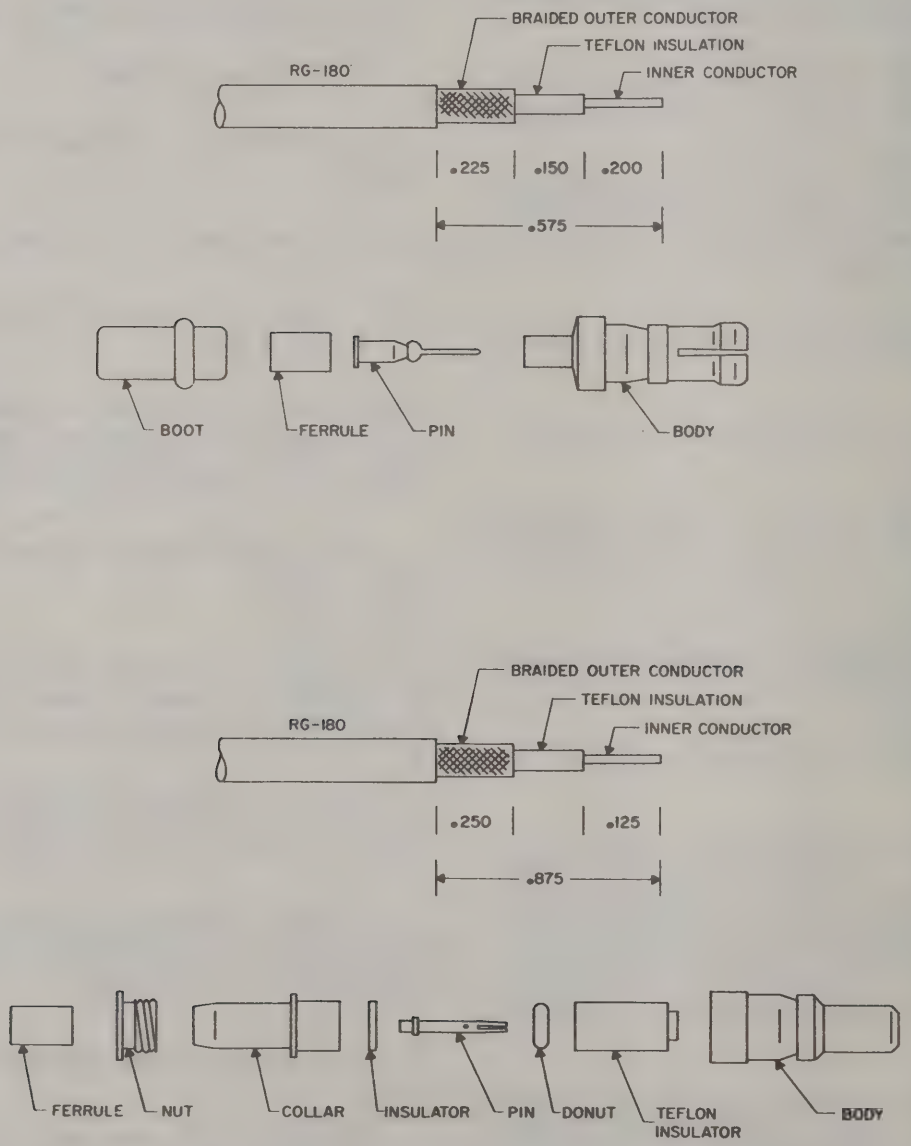


Figure 5–2. Repair of coaxial cable RG–180.

(13) Insert socket into connector W2P1 until it clicks into place.

b. Cable W2P2 Coaxial Cable RG–180 Repair (B fig. 5–2).

(1) Use extractor tool (Bendix part No. 11–8154–1) to remove socket (Bendix part No. 21–33012–24) from connector W2P2.

(2) Cut coaxial cable as close to the socket as possible, insuring that the cut is square.

(3) Slide the ferrule onto the cable.

(4) Slide the nut onto the cable, insuring that the threaded side of the nut is toward the end of the cable.

(5) Strip 0.875 inch outer insulation from the cable to expose the double braided outer conductor.

(6) Cut the double braided outer conductor 0.350 inch from the end of the cable.

(7) Flair the double braided outer conductor slightly, enough to pass over the body of the collar.

(8) Insert the teflon insulation through the collar, ensuring that the double braided outer conductor passes over the outside of the collar, but does not extend byond the ridge.

(9) Trim the teflon insulation flush and squarely at the end of the collar to expose the inner conductor.

(10) Insert the insulator over the inner conductor until it is flush with the end of the collar.

(11) Tin the inner conductor and the inside of the base (ridged end) of the pin, and, while maintaining heat on pin, insert the inner conductor into the base of pin. Allow to cool.

(12) Insert the teflon insulator, with the tip to front, into the base of the body.

(13) Place the rubber donut into the base of the body, and seat it by gently pressing it into place with a small screwdriver.

(14) Insert the pin through the rubber donut into the teflon insulator.

(15) Slide the nut into position and screw it firmly into the body.

(16) Slide the ferrule into position against the nut and use crimping (Thomas and Betts part No. WT230) to crimp ferrule.

(17) Insert pin into connector W2P1 until it clicks into place.

5-19. Intermittents

a. If the operation of a module is intermittently faulty, the trouble may be difficult to locate when the intermittent component is functioning normally. Such troubles can often be found by lightly tapping each part in the suspected portion of the module with a nonmetallic pencil or insulated rod while observing for abnormal operation. If the system continues to function normally, repeat the tapping process at adjoining areas until abnormal operation occurs.

b. Intermittent operation can be caused by loose connections, broken wires, parts with internal defects (including integrated circuits), or dirty contacts on printed wiring cards.

5-20. Power Short Circuits

The IFF set power circuits contain five circuit breakers, one on the control box, the power control panel, the processor, the synchronizer, and the receiver transmitter. When a power short circuit occurs, an associated power circuit breaker will trip to the OFF position. When this occurs the FAULT indicator lamps cannot be used to isolate the defective module. To isolate the component which has a power short circuit, proceed as follows:

a. If the POWER circuit breaker which continuously trips to the OFF position is located on the power control panel or on the control box refer to TM 11–5895–687–12, paragraph 5–12. If the procedures isolate the power short circuit to the interrogator group case proceed to *b* below. If the procedures isolate the power short circuits to an assembly of the interrogator group proceed to *c* below.

CAUTION

During the following procedures (*b* through *d* below) insure that the control box POWER circuit breaker is set to the OFF position before removing or replacing an assembly or a module.

NOTE

When removing and replacing assemblies or modules, refer to TM 11–5895–687–12, paragraphs 5–15, 5–16, and 5–17.

b. To isolate a power short circuit when the power control panel POWER circuit breaker continuously trips to the OFF position, proceed as follows:

(1) Remove the processor, synchronizer and receiver-transmitter assemblies from the interrogator group case.

(2) Set power control panel and control box POWER circuit breaker to the ON positions. If the power control panel POWER circuit breaker trips to the OFF position, the power short circuit is in the interrogator group case wiring. If the power control panel POWER circuit breaker remains in the ON position, set power control panel and control box POWER circuit breakers to OFF and proceed to (3) below.

(3) Install the processor, synchronizer, and receiver-transmitter assemblies into the interrogator group case, one at a time. As each assembly is installed, set the assembly POWER circuit breaker to the ON position and set the power control panel and control box POWER circuit breakers to the ON position. If either the power control panel POWER circuit breaker or the assembly POWER circuit breaker do not remain in the ON position, the power short circuit is in the last installed assembly.

c. To isolate a power short circuit to a module or to the assembly chassis of the suspected assembly, proceed as follows:

(1) Remove all modules from the assembly.

(2) Set the assembly POWER circuit breaker to the ON position.

(3) Set the power control panel and the control box POWER circuit breakers to ON. If the power control panel POWER circuit breaker trips to the OFF position, the power short circuit is in the assembly chassis. If the power control panel POWER circuit breaker remains in the ON position, proceed to (4) below.

(4) Install the modules in the assembly one at a time. Each time a module is replaced, set the assembly POWER circuit breaker and control box POWER switch to the ON position. If the assembly POWER circuit breaker trips to the OFF position, the power short circuit is in the last replaced module.

d. To isolate a power short circuit to a module chassis or to a card within the module, proceed as follows:

(1) With the module installed, remove all cards from the module.

(2) Set the assembly POWER circuit breaker to the ON position.

(3) Set the power control panel and control box POWER circuit breakers to ON. If the assembly POWER circuit trips to the OFF position, the power short circuit is in the module chassis. If the assembly POWER circuit breaker remains in the ON position, proceed to (4) below.

(4) Install the cards into the module one at a time. Each time a card is replaced, set the assembly power circuit breaker to the ON position. If the assembly POWER circuit breaker trips to the OFF position, the power short circuit is in the last replaced card.

5-21. Transistor Testing

The following chart lists the out-of-circuit Beta readings of transistors used in the IFF set as measured with the TS–1836A/U. All Ico readings are less than 0.5 microampere when measured with the TS–1836A/U.

Transistor	Class	Beta	
		Min β	Nominal β
A2292	NPN	60	66
K3502	NPN	68	70
2N861	PNP	30	40

Transistor	Class	Beta Min β	Beta Nominal β
2N2060B (1, 2, 3)	Dual NPN	68	78
2N2060B (4, 5, 6)		68	78
2N2219	NPN	190	205
2N2222	NPN	180	223
2N2222A	NPN	145	161
2N2369A	NPN	80	95
2N2848	NPN	55	75
2N2905	PNP	140	142
2N2905A	PNP	170	210
2N2907	PNP	145	152
2N2907A	PNP	140	152
2N3013	NPN	48	54
2N3019	NPN	140	150
2N3137	NPN	43	46
2N3227	NPN	130	147
2N3265	NPN	70	110
2N3448	NPN	72	82
2N3498	NPN	68	85
2N3500	NPN	120	137
2N3546	PNP	48	62
2N3634	PNP	75	83
2N3719	PNP	57	71
2N3734	NPN	70	95
2N3791	PNP	150	187
2N3792	PNP	135	158
2N3810 (1, 2, 3)	Dual PNP	105	128
2N3810 (4, 5, 6)		105	128
2N3866	NPN	58	78
2N4236	PNP	45	125
2N4910	NPN	47	50

5-22. Removal and Replacement of Conformal Coating

Components mounted on printed wiring cards are covered with a conformal coating. This conformal coating is a protective plastic 0.008 inch ±0.004 which is applied in accordance with MIL–C–46058 (EL) Coatings, conformal (for coating print assemblies)). To remove and replace conformal coating, proceed as follows:

a. Removal of Conformal Coating.

(1) Mount the printed wiring card securely in a work positioning vise or holding jig.

(2) Use soldering Iron, Electrical TL–705/U (tip temperature controlled) with conformal coating stripping tip.

CAUTION

A temperature lower than 525°F will not effectively strip the conformal coating material, and a temperature higher than 550°F will damage the printed wiring on the printed wiring card.

(3) Install heat sinks between area to be worked and components connected to the area to be worked. This may be done using long nose pliers or, when available, use thermal shunts. If a heat sink cannot be installed, do not heat the area being worked longer than 10 seconds at a time, allowing a 30 second cooling period for each 10 seconds worked.

(4) Hold the soldering iron tip at approximately 45° degree angle with the conformal coating to be removed.

(5) Apply a firm gently pushing action into the conformal coating, starting from the middle of the area to be worked and working toward the terminal area. Repeat this action until the conformal coating is removed. Do not attempt to remove the conformal coating in one pass; the area being worked can be easily damaged through abrasion or nicking.

(6) Brush or burnish the area from which the conformal coating was removed before attempting any soldering or recoating operation.

b. Replacing of Conformal Coating. Recoat the repaired area with conformal coating material contained in Repair Kit, Conformal Coating MK–772/U. The conformal coating should be 0.004 inch thick ± 0.002.

c. For more detail in removal and replacement of conformal coating, refer to TB SIG 222.

5-23. Soldering Techniques

Use of correct soldering techniques as described in TB SIG 222 (Solder and Soldering) will greatly reduce the possibility of damage to the part being replaced or repaired. Use of poor soldering techniques will only add to the amount of work the repairman must do.

a. Removing Parts. When removing parts the following techniques are to be used.

(1) Remove conformal coating (para 5–22) and thoroughly clean area to be worked.

(2) Note position of part to be removed and lead connections. For multiconnector parts, a simple diagram of part and leads will assist the repairman in replacing the part, especially if the repairman is not the same as the one who removed the part.

(3) Use Soldering Iron, Electrical TL–705/U which has tip temperature control. Use 60/40 rosin core solder which becomes liquid when heated above 374°F.

(4) Heat the soldering iron to the desired temperature and tin the tip with a small amount of 60/40 rosin core solder. A well tinned soldering iron tip provides for quick transfer of heat.

(5) When unsoldering transistors and diodes install a heat sink or thermal shunt between the part and the soldered area.

(6) Heat the soldered area quickly and as soon as the solder becomes liquid, remove it with a solder syringe.

(7) Make sure that all solder has been removed before attempting to remove the part.

b. Replacing Parts. When replacing parts the following techniques are to be used.

(1) Prepare the soldering iron as described in *a* (4) above.

(2) Trim the leads of the replacement part, where necessary, and bend the leads to fit the area in which they are to be soldered.

(3) Lightly tin the leads of the part and place it in position.

(4) Use the minimum amount of solder required to make the connection. Use a heat sink between the part and the soldering area.

(5) Remove the solder before removing the soldering iron.

NOTE

A solid solder joint appears bright, shiny, and smooth. A poor or cold solder joint appears frosty gray and crystaline.

5-24. Repair of Printed Wiring

Repair of printed wiring consists of repair of small or large delaminated areas, and gouged or cracked printed wiring. These repairs are described in TB SIG 222 C1 (Solder and Soldering).

a. Repair of Small Delaminated Areas. To repair a small (less than one inch) delaminated area, proceed as follows:

(1) Remove the conformal coating from the area to be repaired (para 5–22).

(2) Apply a heavy layer of the bonding agent, contained in Repair Kit MK–772/U, around the delaminated area and allow the bonding agent to flow under the printed wiring.

CAUTION

Do not force the bonding agent under the printed wiring because this will cause further delamination.

(3) Allow the bonding agent to become tacky (approximately 15 minutes).

(4) Gently press the printed wiring against the baseboard and allow the bonding agent to cure for 1½ hours at room temperature.

(5) Replace conformal coating (para 5–22).

b. Repair of Large Delaminated Areas. To repair a large (greater than an inch delaminated area), proceed as follows:

(1) Remove the conformal coating from the area to be repaired.

(2) Cut away the delaminated section of printed-wiring with a sharp knife or razor blade (being careful not to cut or gouge the baseboard) and clean the ends of the printed-wiring to obtain a clean surface for solering.

(3) Obtain a piece of wire ribbon, contained in Repair Kit MK–772, or an identical section of the printed wiring from a throw away printed wir-

ing card and cut the wire ribbon or section of printed wiring to fit against the baseboard with 1/8 inch overlap on the printed wiring.

(4) Hold the wire ribbon or section of printed-wiring in place with a nontinnable scribe and solder each end to the printed wiring with 1/32-inch diameter 60/40 rosin core solder.

CAUTION

Do not apply heat to the printed wiring for longer than 8 seconds. Excessive heat will cause further delamination. If soldering operations exceed the time limits, allow a 30-second cooling period before continuing the soldering operation.

(5) Perform steps in *a* above to laminate the new printed wiring to the board.

c. Repair of Gouges and Scratches. Repair of gouges and scratches in printed wiring may be accomplished by removal of the conformal coating (para 5-22), bridging the gouge or scratch with solder and replacing the conformal coating.

d. Repair of Deep Gouges and Cracks. To repair deep gouges and cracks in printed wiring, proceed as follows:

(1) Remove the conformal coating (para 5-22).

(2) Clean the printed wiring conductor surface to obtain a clean surface for soldering.

(3) Cut a piece of wire ribbon, contained in Repair Kit MK-772/U, approximately one quarter inch long.

(4) Hold the wire ribbon in place with a nontinnable scribe, centered over the crack or gouge, and solder the wire ribbon to the printed wiring with 1/32-inch diameter 60/40 rosin core solder.

(5) Replace the conformal coating (para 5-22).

5-25. Hot Mock-up for the IFF Set

The hot mockup configuration of the IFF set provides a realistic system test bed for troubleshooting, testing, and aligning of assemblies, modules, and cards. The hot mockup configuration requires the use of components of Test Facility Set AN/TPM-24(V)3 to extend the assemblies from the interrogator group case and to extend cards from the modules. To set up the hot mock-up configuration, refer to figure 5-3 and perform the following steps, as applicable:

NOTE

The hot mockup configuration, described below, shows all assemblies extended from the interrogator group case. This configuration may be altered to extend any one or two assemblies, as required. Any assembly not required for a specific troubleshooting procedure should not be extended from the interrogator group case.

a. Remove all power from the IFF set by setting the power control panel and control box POWER circuit breakers to their OFF positions.

b. Remove the required assembly(s) from the interrogator group case (refer to TM 11-5895-687-12, para 5-15).

NOTE

Unless otherwise indicated, all cables referred to in the following steps are contained in the AN/TPM-24(V)3.

c. Assemble the test equipment and make the following connections:

(1) Connect cable W43P1 to connector 1A1P1 on the processor assembly and W43P2 to connector 1XA1P1 in the interrogator group case.

(2) Connect cable W41P1 to connector 1A2P1 on the synchronizer and W41P2 to connector 1XA2P1 in the interrogator group case.

(3) Connect cable W42P1 to connector 1A2P2 on the synchronizer and W42P2 to connector 1XA2P2 in the interrogator group case.

(4) Connect cable W39P1 to connector 1A3P1 on the receiver-transmitter and W39P2 to connector 1XA3P1 in the interrogator group case.

(5) Connect cable W40P1 to connector 1A3P2 on the receiver-transmitter and W40P2 to connector 1XA3P2 in the interrogator group case.

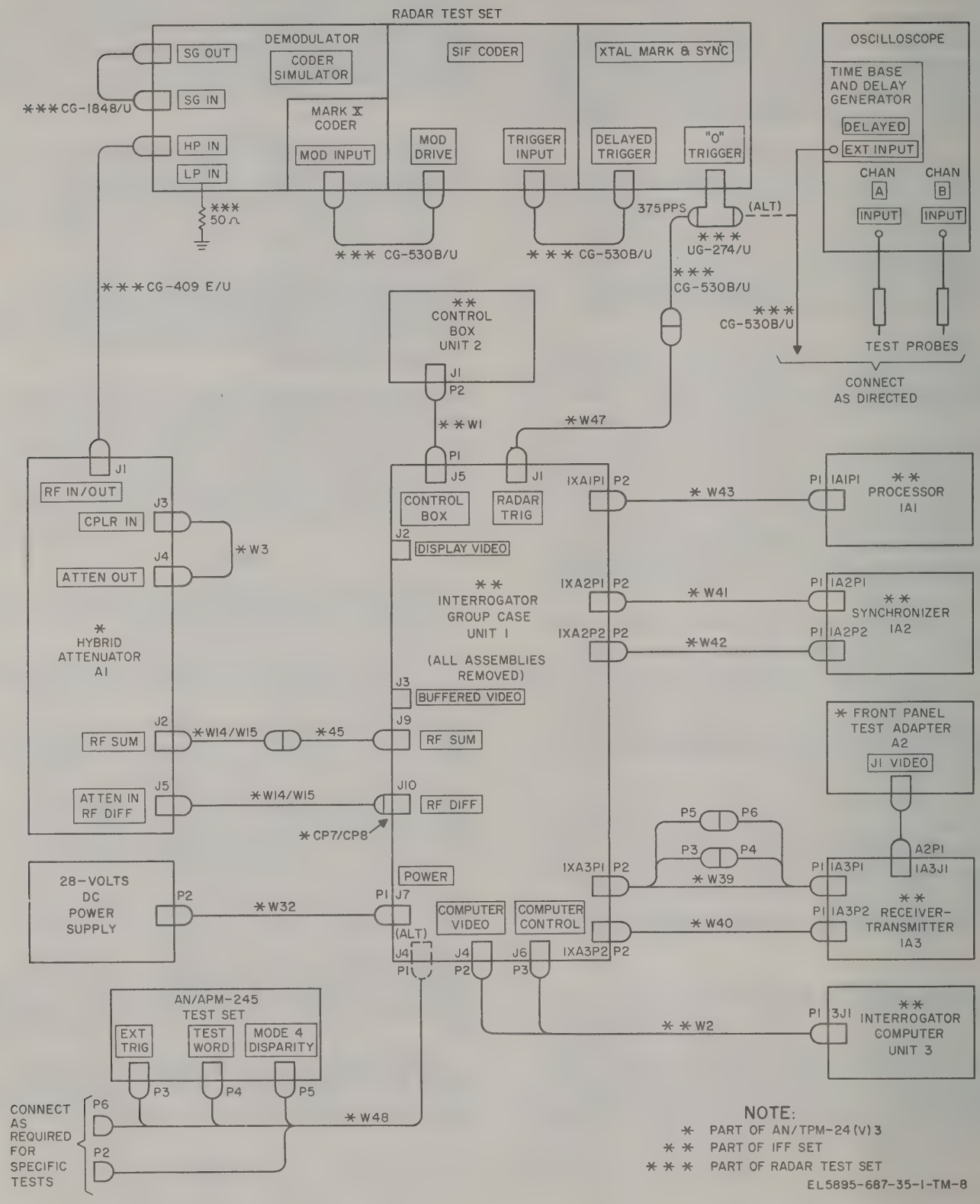


Figure 5-8. Hot mockup configuration for the IFF set.

(6) If the interrogator computer is to be used proceed to (*a*) below. If the AN/APM–25 test set is to be used proceed to (*b*) below.

(*a*) Connect IFF set cable connectors W2P2 and W2P3 to COMPUTER VIDEO jack J4 and COMPUTER CONTROL jack J6, respectively, on the interrogator group case, and W2P1 to connector J1 on the interrogator computer.

(*b*) Connect cable W48P1 to COMPUTER VIDEO jack J4 on the interrogator group case, and connectors W48P3, W48P4, and W48P5 to TRIG, TEST WORD, and MODE 4 DISPARITY jacks, respectively, on the AN/APM–25 test set. Connectors W48P2 and W48P6 are to be connected as required in the test procedures.

(7) Connect cable connectors W32P1 to POWER jack J7 on the interrogator group case, and W32P2 to the 28-volt dc power supply.

(8) Connect the two W14/W15 cables, cable W45 and adapter CP7/CP8 between the interrogator group case and the hybrid attenuator (part of the AN/TPM–24), as follows:

(*a*) Connect adapter CP7/8 to RF DIFF jack J10 on the interrogator group case.

(*b*) Connect one cable W14/W15 between adapter CP7/CP8 and ATTEN IF RF DIFF jack J5 on the hybrid attenuator.

(*c*) Connect cable W45 between RF SUM jack J9 on the interrogator group case, and to the other cable W14/W15.

(*d*) Connect the opposite end of cable W14/W15 to RF SUM jack J2 on the hybrid attenuator.

(9) Connect IFF set cable W1P1 to CONTROL BOX jack J5 on the interrogator group case, and W1P2 to jack J1 on the control box.

(10) Connect cable W47 between RADAR TRIG jack J1 on the interrogator group case and a length of radar test set cable CG–530B/U (62 inch). The opposite end of this cable connects to a radar test set UG–274/U connector adapter which is installed on the "O" TRIGGER jack on the radar test set.

(11) Connect radar test set cable CG–530 B/U between the DELAYED TRIGGER and TRIGGER INPUT jacks on the radar test set.

(12) Connect radar test set cable CG–530B/U (9-3/8 inch) between the MOD DRIVE and MOD INPUT jacks on the radar test set.

(13) Connect radar test set cable CG–1848/U (6-1/8 inch) between the SG IN and SG OUT jacks on the radar test set.

(14) Connect radar test set cable CG409E/U between the HP IN jack on the radar test set and RF IN/OUT jack J1 on the hybrid attenuator. Terminate LP IN jack with terminating plug DA232/U.

(15) Connect cable W3 (tied to hybrid attenuator) between CPLR IN jack J3 and ATTEN OUT jack J4 on the hybrid attenuator.

(16) Normally the oscilloscope SYNC IN jack will be connected to the "O" TRIGGER jack on the radar test set with radar test set cable CG–530 B/U (62 inch) although, special test procedures may require connection to a test point within the IFF set.

d. The hot mockup is now complete. Apply power to the radar test set, the oscilloscope, the word generator, and the 28-volt dc power supply as outlined in their respective operators manuals. Apply power to the IFF set as outlined in TM 11–5895–687–12 paragraph 2–11.

Section II.

TOOL AND TEST EQUIPMENT REQUIRED FOR DS, GS, AND DEPOT MAINTENANCE OF INTERROGATOR SET AN/TPX-50

5-26. Tools Required

Tools are not supplied with the IFF set; however, the following tools are required for ds, gs, and depot maintenance.

Quantity	Tool	Literature
1	Tool Kit, Electronics Equipment TK-100/G.	SC 5180-91-CL- S21
1	Tool Kit, Electronics Equipment TK-105/G	
	Tools, Extraction, Insertion and Crimping.	
1	Tool, extraction Bendix 11-7880-16.	
1	Tool, extraction Bendix 11-7880-20.	
1	Tool, extraction Amp 294-238.	
1	Tool, extraction Bendix 11-8154-1.	
1	Tool, crimping MS 3191-1 with MS 3191-16A and MS 3191-20A dies.	
1	Tool, crimping Thomas and Betts WT 403.	
1	Tool, crimping Thomas and Betts WT 230.	
1	Tool, insertion Bendix 11-7401-16.	
1	Tool, insertion Bendix 11-7401-20.	

5-27. Additional Test Equipment Required

Test equipment is not supplied with the IFF set, however, the following test equipment is required for ds, gs, and depot maintenance of the complete AN/TPX-50. The list also references the assigned common name and the literature for the equipment.

Test equipment	Common name	Literature
Test Set AN/UPM-98A	Radar test set	TM 11-6625-403-15-1
Test Set AN/APM-245A	Word generator	T.O. 33A1-8-468-1/ TM 11-6625-1711-15-1
Generator, Signal AN/URM-49.	Signal generator	TM 11-6625-280-15
Generator, Signal AN/URM-64A	RF signal generator	TM 11-6625-299-15
Slotted Line, Coaxial IM-92/U.	Slotted Line	TM 11-5109
Indicator, Standing Wave, Ratio AN/UPM-108A.	Swr indicator	TM 11-6625-335-12
Dummy Load Electrical DA-265/U.	Dummy Load	
Oscilloscope AN/USM-281A	Oscilloscope*	TM 11-6625-1703-15
Multimeter AN/PSM-6B.	Multimeter*	TM 11-6625-475-10
Voltmeter, Electronic ME 202A/U.	Voltmeter*	TB 9-6625-1338-50
Generator, Sweep Signal AN/USM-203A	Sweep generator	TM 11-6625-2575-14
Heat Gun, Master Appliance Model HG-501L	Heat gun*	9-4940-465-12
Frequency Meter TS-186D/UP.	Frequency meter	TM 11-2691-15
Wattmeter AN/URM-98A	Wattmeter	TM 11-6625-433-15
Counter, Electronic, Digital Readout AN/USM-207A	Counter	NAVSHIPS 0969-125-0010 NAVSHIPS 0969-125-0020
Attenuator Fixed 10db, CN-1024/U.	10db attenuator	
Attenuator Fixed 6 db.	6 db attenuator	
Attenuator Fixed 3 db.	3 db attenuator	
Coaxial Tuner, FXR-S102N.	Coaxial tuner	
Power Supply PP-2953A/U	28-volt dc power supply	TM 11-6130-233-12
Test Facilities Set AN/TPM-24/(V)3	Test facility set*	TM 11-6625-2398-15-3
Repair Kit, Printed Wiring Board MK-772/U.	Repair kit*	

*Items required for procedures in this manual

CHAPTER 6

TROUBLESHOOTING BASED ON STARTING PROCEDURE

1. General

.e troubleshooting chart based on starting pro-dure (para 6–5) is designed to enable the repair-an to locate trouble based on indications ob-ined while starting the equipment, and is per-rmed with the equipment installed on-line (in)eration with the associated radar). It will aid in :tecting abnormal operation of the IFF set and in :ating faulty parts that cause abnormal operation f the IFF set and in locating faulty parts that ause abnormal operation.

a. Follow the step-by-step starting procedure vhile carefully observing the *Normal indications* isted for each step.

b. If the normal indications are not obtained, check the *Abnormal indications* column for the particular abnormal indications obtained.

c. Perform the checks given in the *Corrective measures* column for the particular abnormal indications obtained.

d. When it is required that assemblies be extended to make checks, refer to paragraph 5–25 for necessary AN/TPM–24 extender cable connections.

e. For necessary removal and replacement procedures, see TM 11–5895–687–12.

6-2. Reference Data

The following data will be helpful to the repairman who is using the troubleshooting chart based on starting procedure to troubleshoot the IFF set.

Reference	*Data*
Figure 6–1	Interrogator group case, power control panel, rear view.
Figure 6–2	Control box panel, rear view.
Figure 6–3	Interrogator group case, inside rear of group case, viewed through processor opening.
Figure 6–4	Interrogator group case, power control panel and internal connectors.
Figure 6–5	Troubleshooting waveforms.
Figure 12–3	IFF set interconnection diagram.
Figure 12–4	Control circuits, functional block diagram (including power distribution)
Chapter 4	Control circuit functioning, including power distribution.

6-3. Fuses and Interlocks

a. Fuses. There are no fuses in the IFF set. All power control switches are circuit breakers.

b. Interlocks. There are no interlocks in the IFF system.

6-4. Preliminary Checks and Control Settings

a. Additional damage may be caused if power is applied to equipment in which a complete or partial short circuit exists. When any of the following conditions applies, check for short circuits before applying power to the IFF set.

(1) A circuit breaker that will not remain in the ON position.

(2) Smoke observed coming from a component

(3) Overheated parts located by observation or the sense of smell.

(4) A defective component being serviced in another unit used with but not a part of the IFF set, where the nature of the trouble is not known.

(5) Abnormal symptoms reported from operational tests indicating possible partial or complete short circuits.

b. Before using the troubleshooting chart based on starting procedure (as explained in para 6—1), check with the operator for indications that would show the location of trouble. Refer to TM 11–5895–687–12 for the locations of the following switches and circuit breakers and set them as directed. The XMTR MOD switch, the last listed, is located on the receiver-transmitter chassis behind front panel connector J1 TEST. All indicator lamps should have their shutters set in their counterclockwise (bright) positions. Necessary switches of the associated radar have been activated to supply +28 vdc to the IFF set.

NOTE

Switches on the control box that are not listed have spring-loaded positions.

Switch or circuit breaker	*Position*
Control box unit 2:	
POWER	OFF
PANEL	DIM
CODE SELECT subassembly:	
MODE 1	Test code (any code will do)
MODE 2	Test code (any code will do)
MODE 3/A	Test code (any code will do)
GTC	ON
PROCESSOR	IN
MODE 4	A or B as required for operation
MODE SELECT	As required for operation
Interrogator group unit 1 control panel:	
POWER	OFF
Processor 1A1	
POWER	OFF
METER	OUT
Synchronizer 1A2:	
POWER	OFF
Power supply test switch	OUT
Receiver-transmitter 1A3:	
POWER	OFF
RF POWER SWITCH	As required for operation
Internal switch	
XMTR MOD	ON

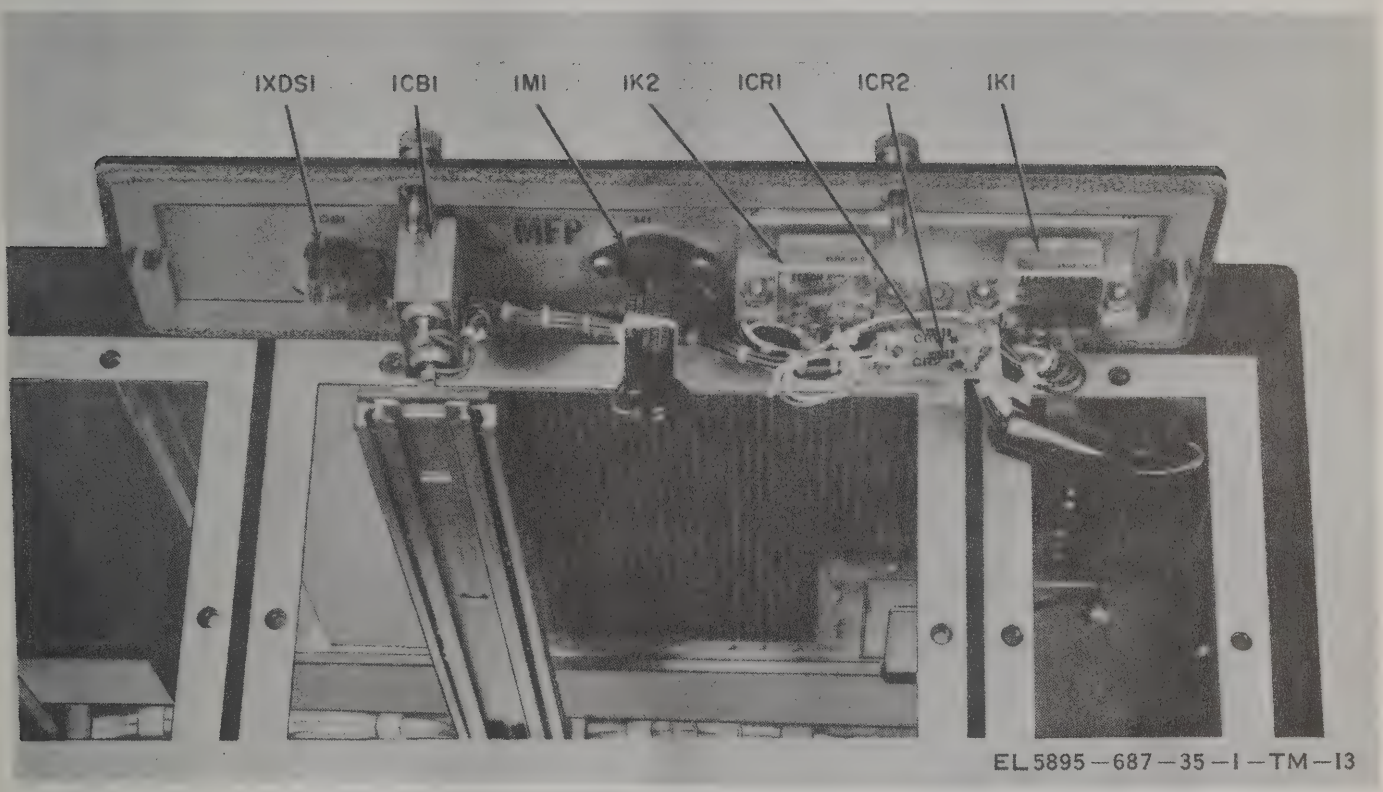


Figure 6–1. Interrogator group case, power control panel, rear view.

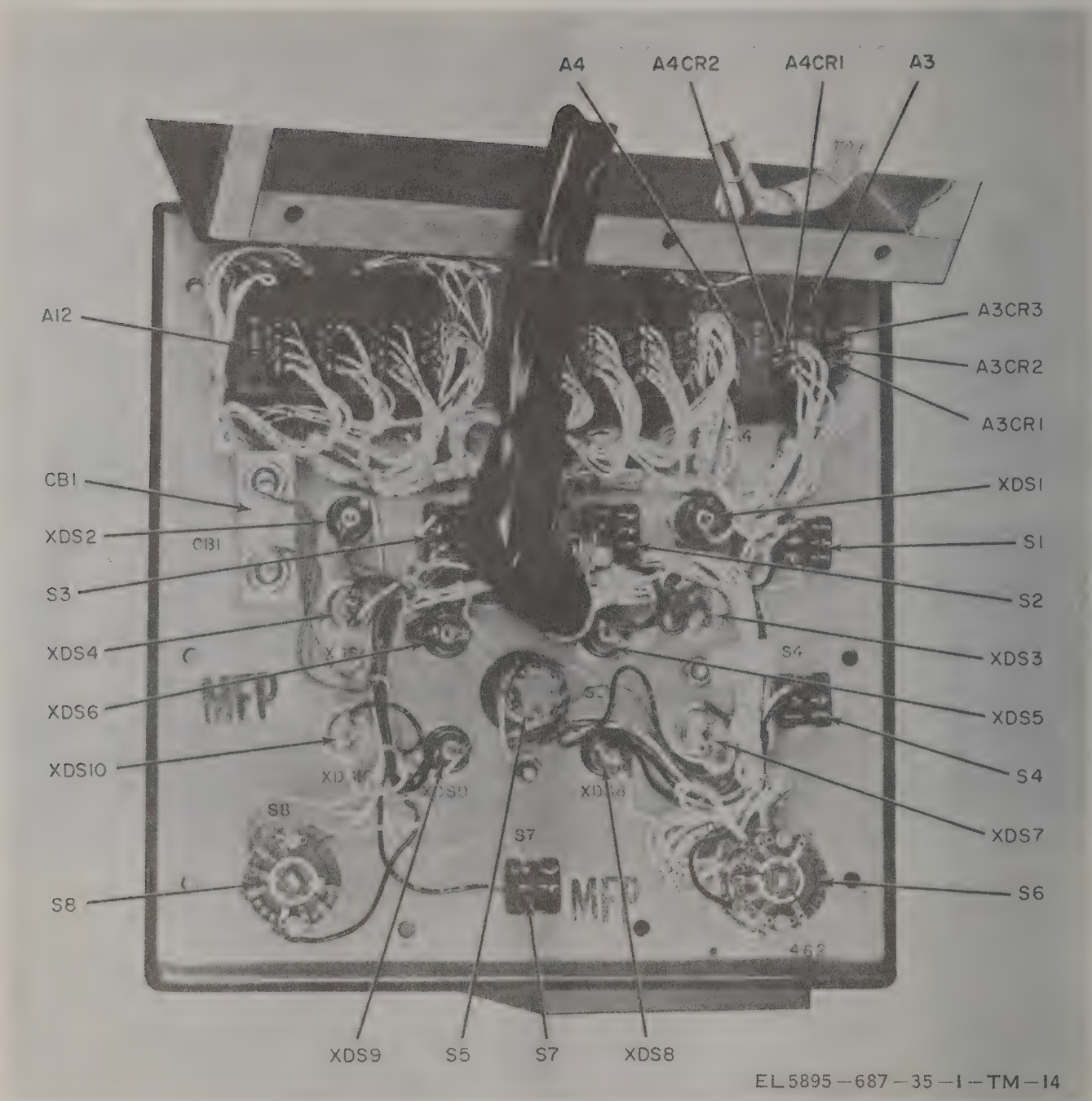


Figure 6–2. Control box panel, rear view.

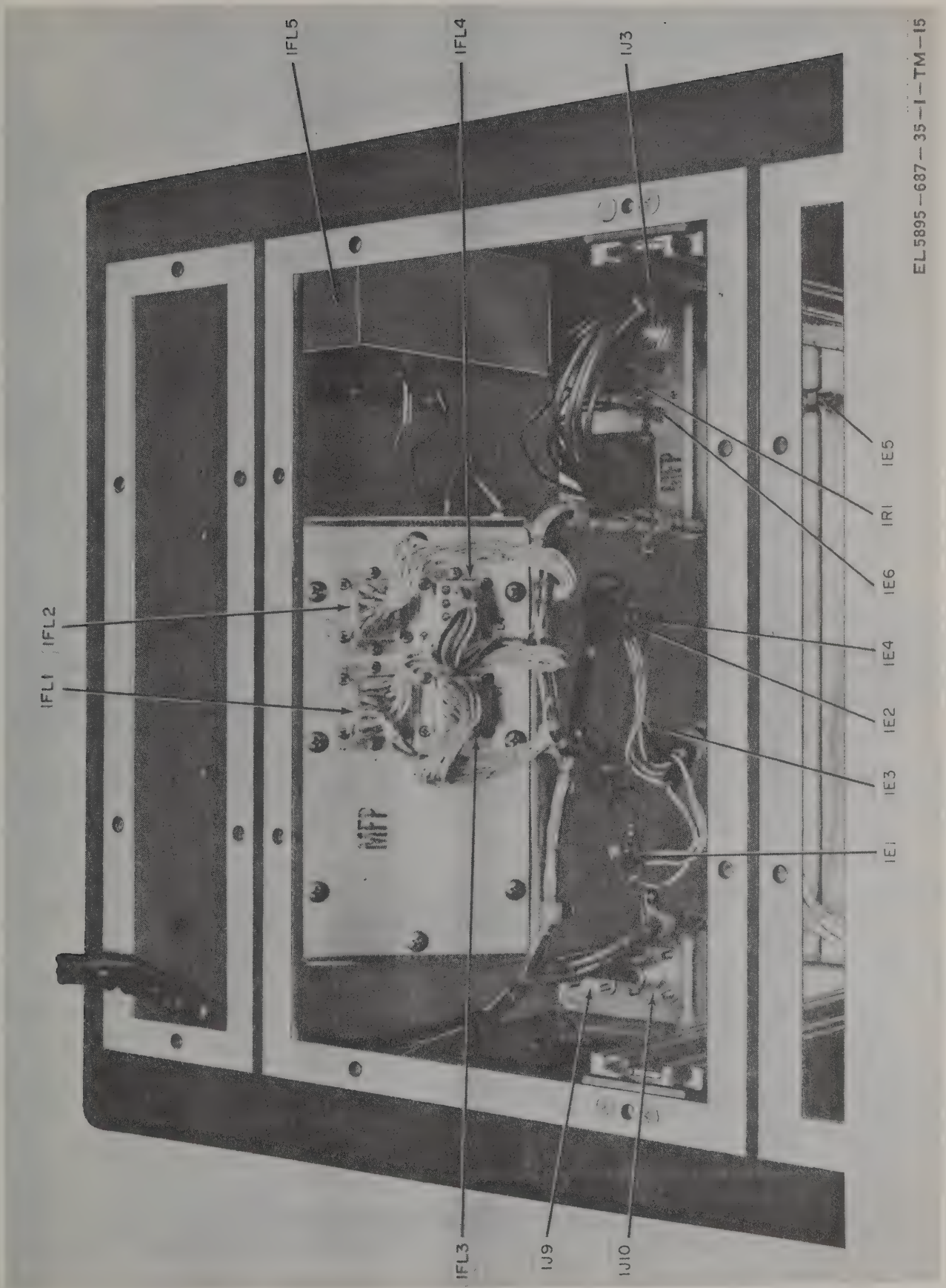


Figure 6-3. Interrogator group case, inside rear of group case, viewed through processor opening.

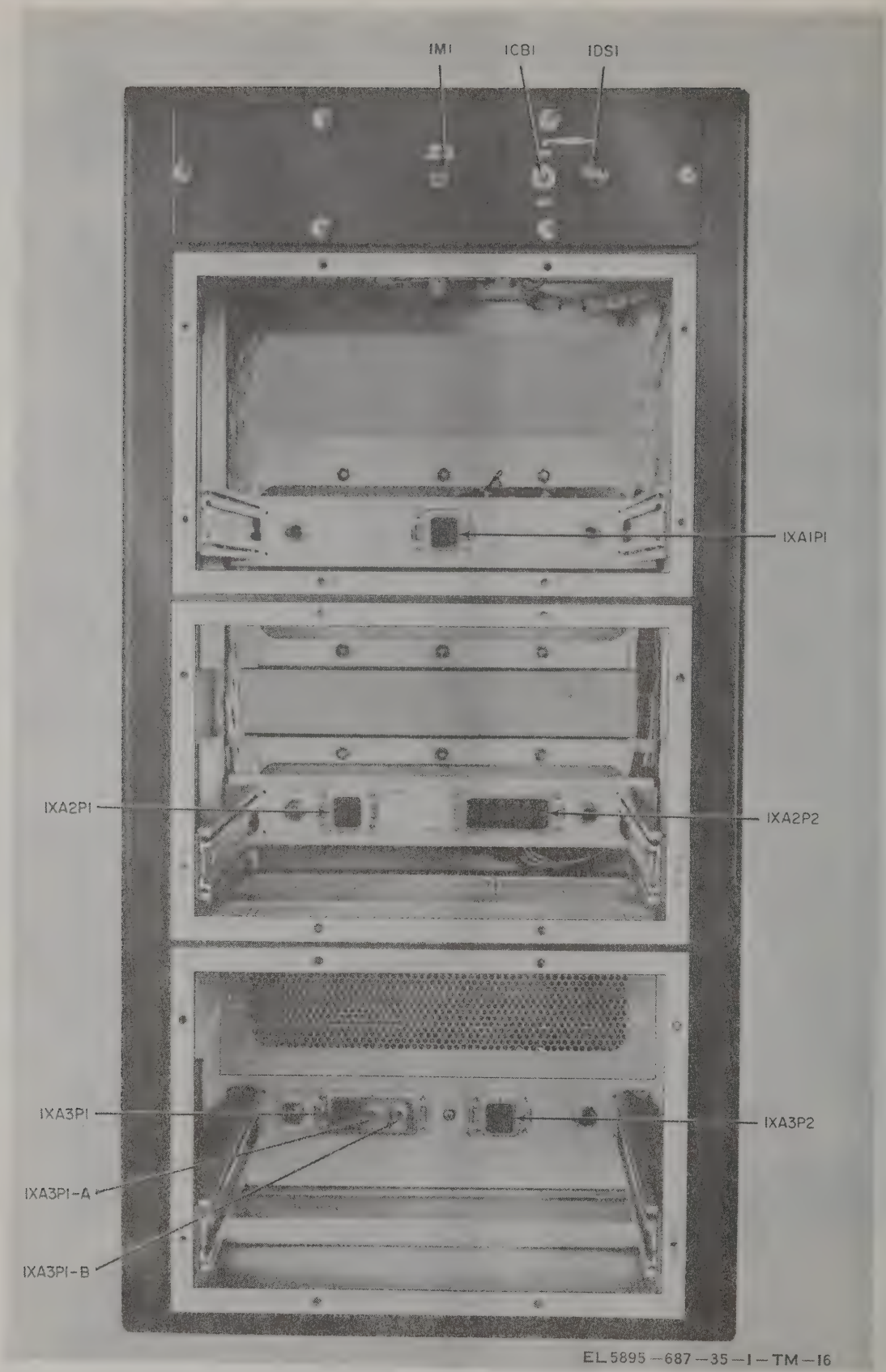


Figure 6–4. Interrogator group case, power control panel and internal connectors.

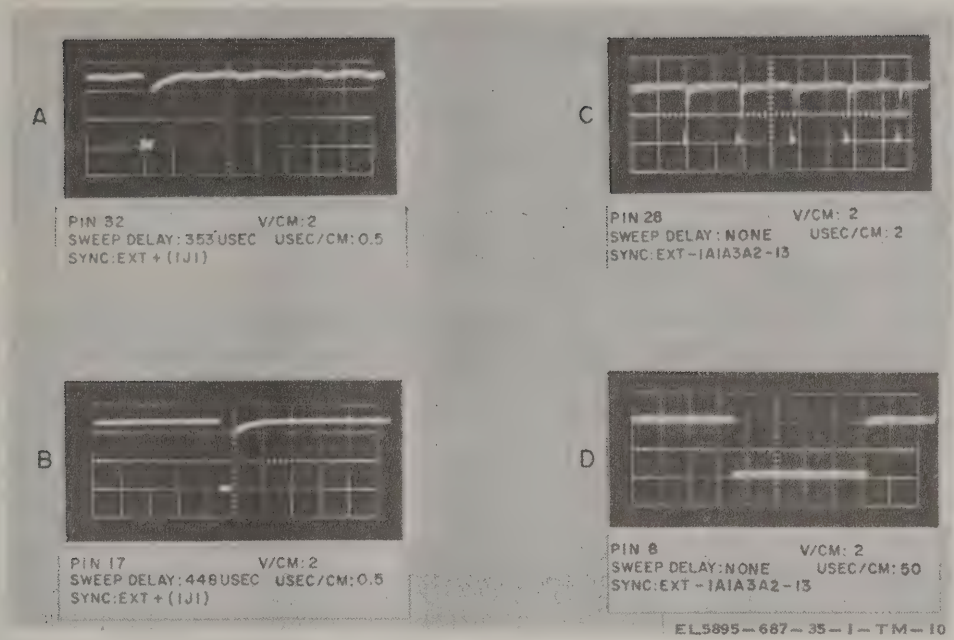


Figure 6–5. Troubleshooting waveforms.

6-5. Troubleshooting Chart Based on Starting Procedure

NOTES

1. SELF TEST fault indicator lamps on the control box light whenever the self-test circuits in the IFF set detect faults. The lamps also light if the interrogator computer or an assembly in the interrogator group is not energized, if the initial 60–second time delay in the receiver-transmitter has not elapsed, or if a code has not been set in the interrogator computer. During the following procedures some fault indications will be present until the last assembly has been energized.

2. If after all initial fault conditions have been allowed to stabilize, two or more SELF TEST fault lamps remain lit simultaneously, set the PROCESSOR switch to BYPASS and the MODE SELECT to any sif mode. Then check the assemblies indicated by the lighted lamps in the following order of preference: synchronizer, KIR, receiver-transmitter, processor.

3. Once set to ON, POWER circuit breakers 1CB1 and 2CB1, unless otherwise directed, shall remain in the ON position for the entire procedure.

4. During the following procedures, extender cables from Test Facilities Set AN/TPM–24(V)3 must be used to extend the processor, synchronizer and receiver-transmitter from the interrogator group case. To make these connections, as necessary, refer to paragraph 5–25 and figure 5–2.

Step	Procedure	Normal indications	Abnormal indications	Corrective measures
1	Switches set as in para 6–4*b*. Code inserted in interrogator computer. Power and radar triggers are being supplied by associated radar. Momentarily depress POWER indicator lamp 1DS1 on the power control panel.	Lamp 1DS1 lights.	Lamp 1DS1 does not light.	Check lamp 1DS1, filter FL5 and capacitor 1C1.

Step	Procedure	Normal indications	Abnormal indications	Corrective measures
2	Set POWER circuit breakers 1CB1 on the power control panel and 2CB1 on the control box to ON.	*a.* Power indicator lamps 1DS1 on the power control panel and 2DS2 on the control box are lighted, and TOTAL HOURS meter 1M1 operates.	*a.* POWER indicator lamps on the control box and power control panel are not lighted, and 1M1 does not operate.	*a.* Check POWER circuit breaker 1CB1, POWER circuit breaker 2CB1, relay 1K1 and diode 1CR1.
		b. PROC, SYN, and R/T SELF TEST fault indicator lamps on the control box light.	*b.* SELF TEST fault indicator lamp 2DS5, 2DS8, or 2DS9 does not light.	*b.* Depress LAMP TEST switch 2S5. SELF TEST fault indicator lamps 2DS5, 2DS8, 2DS9, CHALLENGE indicator lamp 2DS1, and POWER lamp 2DS2 should light. (1) If all lamps light, check enable (ground) input and associated lamp driver on lamp driver card 2A1 for lamp that did not light in *b* above. (2) If lamp does not light when LAMP TEST switch is depressed, replace lamp.
		c. KIR SELF TEST indicator lamp is out.	*c.* KIR SELF TEST indicator lamp is lit.	*c.* Interrogator computer is at fault. Could be low randomness condition; if permitted (para 4–7*b*(2) (b), note), try LOCKOUT OVERRIDE position of MODE SELECT switch 2S6. (1) If SELF TEST lamp goes out, it was low randomness. (2) If SELF TEST lamp stays on, it is some other interrogator computer fault.
3	On the synchronizer, momentarily depress POWER indicator lamp 1A2DS5.	POWER indicator lamp 1A2DS5 lights.	POWER indicator lamp does not light.	Check POWER indicator lamp 1A2DS5. *a.* If lamp is good, check for +28 vdc at pin 1 and then pin 3 of filter 1A2A6. (See note 4.) *b.* If +28 vdc is at pin 1 but not at pin 3, filter 1A2A6 is defective. Refer to TM 11–5895–687–35–3.

Step	Procedure	Normal indications	Abnormal indications	Corrective measures
4	Set POWER circuit breaker 1A2CB1 on the synchronizer to ON.	*a.* POWER indicator lamp 1A2DS5 lights. *b.* One or more FAULT indicator lamps may light briefly and then go out.	*a.* POWER indicator lamp does not light. *b.* FAULT indicator lamp does not go out.	*a.* Check synchronizer circuit breaker 1A2CB1. *b.* If RADAR TRIG FAULT and SYN SELF TEST lamps stay on, verify that radar trigger appears at 1A2A1A7J4. (A radar trigger is from 3 to 50 volts amplitude with a duration of 0.5 to 20 μsec.) If radar trigger is verified, or if any other fault lamp stays on, refer to TM 11–5895–35–3.
5	Momentarily depress RADAR TRIG FAULT 1A2DS1, TIMING FAULT 1A2DS2, CODER/DECODER FAULT 1A2DS3, and INTERFACE FAULT 1A2DS4 indicator lamps.	All indicator lamps light.	An indicator lamp does not light.	Check lamp and lamp wiring.
6	Check the synchronizer power supply voltage by turning power supply test selector 1A2S1 to the –12, +12, and +5 positions.	Synchronizer assembly meter 1A2M1 should read in the solid green area for all settings of 1A2S1.	Meter does not read in the solid green area.	Refer to TM 11–5895–687–3 for synchronizer power supply module check.
7	On the processor, momentarily depress POWER indicator lamp 1A1DS5.	POWER indicator lamp 1A1DS5 lights.	POWER indicator lamp does not light.	Check POWER indicator lamp 1A1DS *a.* If lamp is good, check for +28 vdc at pin 1 and then pin 3 of filter 1A1A7. (See note 4 above). *b.* If +28 vdc is at pin 1, but not at pin 3, filter 1A1A7 is defective.
8	Set POWER circuit breaker 1A1CB1 on the processor assembly to ON.	*a.* POWER indicator lamp 1A1DS5 lights. *b.* FAULT lamps should not light.	*a.* POWER indicator lamp does not light. *b.* A FAULT lamp stays on.	*a.* Check circuit breaker 1A1CB1. *b.* If lamp does not go out, refer to TM 11–5895–687–35–3.
9	Depress following FAULT indicator lamps: TIMING 1A1DS1, MEMORY 1A1DS2, TARGET 1A1DS3, and FRIEND 1A1DS4.	All indicator lamps light.	An indicator lamp does not light.	Check lamp wiring and lamp.

Step	Procedure	Normal indications	Abnormal indications	Corrective measures
10	Set METER switch 1A1S2 to IN.	METER 1A1M1 reads in solid green area.	METER 1A1M1 does not read in solid green area.	Refer to TM 11–5895–687–35–2 for processor power supply check.
11	Set PROCESSOR switch 2S2 to BYPASS and set and hold CHALLENGE switch 2S1 to TEST.	Correct test target pattern appears on ppi without friend eyelashes.	Incorrect test pattern.	Check for waveforms (A) self-test pretrigger (A, fig. 6–4) at 1A2A1A7–8, (B) processor start pretrigger (B, fig. 6–5) at 1A2A1A7–12, (C) strobe (C, fig. 6–4) at 1A1A3A2–28, and (D) processor self-test gate (D, fig. 6–5) at 1A1A3A3–8. *a.* If all waveforms are present, synchronizer is faulty. Refer to TM 11–5895–687–35–3. *b.* If either of both waveforms (A) and (B) are missing: (1) Set POWER circuit breaker 1A1CB1 on the processor to OFF and disconnect processor from the interrogator group case. (2) Recheck for waveforms (A) and (B). If waveforms are still missing, synchronizer is faulty. Refer to TM 11–5895–687–35–3. If waveforms are present, processor is faulty. Refer to TM 11–5895–687–35–3. (3) Reconnect processor to interrogator group case and set POWER circuit breaker to 1A1CB1 to ON. *c.* If waveforms (C) and (D) are missing: (1) Set POWER circuit breaker 1A2CB1 to OFF, remove card 1A2A1A8 from synchronizer and set POWER circuit breaker 1A2CB1 to ON.

Step	Procedure	Normal indications	Abnormal indications	Corrective measures
				(2) Recheck for waveforms (A) and/or (B). If waveforms are still missing, processor is faulty. Refer to TM 11–5895–687–35–2. If waveforms are present, synchronizer is faulty. Refer to TM 11–5895–687–35–3.
12	Set PROCESSOR switch to IN and set and hold CHALLENGE switch 2S1 to TEST.	Correct test target pattern appears on ppi with friend eyelashes.	Incorrect test pattern.	Refer to TM 11–5895–687–35–2 to check reply processing system.
13	On the receiver-transmitter, momentarily depress POWER indicator lamp 1A3DS4.	POWER lamp 1A3DS4 lights.	POWER lamp 1A3DS4 does not light.	Check POWER indicator lamp 1A3DS4. *a.* If lamp is good, check for +28 vdc at the input and output of filter 1A3FL1. (See note 4.) *b.* If +28 vdc is at the input, but not at the output, filter 1A3FL1 is defective. Refer to TM 11–5895–687–35–4.
14	Set POWER circuit breaker 1A3CB1 on receiver-transmitter to ON.	*a.* POWER lamp 1A3DS4 lights. *b.* RF SWITCH FAULT lamp 1A3DS1 and XMTR FAULT lamp 1A3DS3 may or may not light and go out. RCVR FAULT lamp 1A3DS2 on the receiver-transmitter and R/T SELF TEST lamp 2DS9 on the control box remain lit for approximately 1 minute, then go out. TOTAL HOURS meter 1A3M1 operates.	*a.* POWER lamp does not light. *b.* (1) One or more FAULT lamps do not light at all. (2) RCVR FAULT lamp 1A3DS2, XMTR FAULT lamp 1A3DS3, RF SWITCH FAULT lamp 1A3DS1, or any combination of them, remains on after 60 seconds, or TOTAL HOURS meter does not operate.	*a.* Check circuit breaker 1A3CB1 and associated wiring. *b.* (1) Depress FAULT lamp(s) that do(es) not light. If lamp does not light, replace lamp. (2) Depress FAULT RESET button S1. If a lamp remains lighted, refer to TM 11–5895–687–35–4 for corrective measures.
15	Depress RF SWITCH FAULT 1A3DS1, RCVR FAULT 1A3DS2, and XMTR FAULT 1A3DS3 indicators.	All indicator lamps light.	An indicator lamp does not light.	Replace lamp.
16	Activate challenges in modes 1, 2, and 3/A by setting MODE SELECT switch to mode desired and hold CHALLENGE switch to ON.	CHALLENGE lamp 2DS1 lights.	CHALLENGE lamp does not light.	If CHALLENGE lamp does not light, check all SELF TEST and FAULT lamps. Trouble is associated with the corresponding fault indications.

CHAPTER 7

CONTROL CIRCUITS TROUBLESHOOTING AND REPAIR

Section 1. CONTROL CIRCUITS TROUBLESHOOTING INFORMATION

7-1. Reference Data

The following information will be helpful when troubleshooting and/or repairing the control circuits.

Reference	*Data*
Figure 12–4	Control circuits, functional block diagram.
Figure 12–6	Control box, interconnection schematic diagram (includes error indicator card 2A2).
Figure 12–5	Interrogator group case 1A1, schematic diagram.
Figure 12–7	Lamp driver board 2A1, schematic diagram and component locations.
Figure 12–2	IFF set, system functional block diagram.

7-2. Control Circuits, Controls and Functions

The following chart lists the controls that are functional parts of the control circuits:

Controls	Location	Function
Interrogator group case, unit 1.	Refer to figure 3–2, TM 11–5895–687–12, for location of controls.	
POWER circuit breaker 1CB1 (two-position circuit breaker).		When set to ON, connects +28 vdc to the control box.
POWER indicator lamp 1DS1		Lights when POWER circuit breakers 1CB1 and 2CB1 (on the control box) are set to ON.
TOTAL HOURS meter 1M1		Indicates elapsed time of operation of the IFF set. Operates when circuit breakers 1CB1 and 2CB1 are set to ON.
Control box, unit 2 POWER circuit breaker 2CB1 (two-position circuit breaker).	Refer to figure 3–1, TM 11–5895–687–12, for location of controls.	When set to ON, with 1CB1 on power control panel ON, connects +28 vdc to IFF set (POWER indicator lamps light on control box and power control panel).
POWER indicator lamp 2DS2 (white).		Lights when POWER circuit breakers 1CB1 and 2CB1 are set to ON and +28 vdc is available at IFF set.
PANEL switch 2S3 (three-position toggle, center position OFF).		Controls intensity of edge light and CODE SELECT switch assembly lamps: low at DIM, high at BRIGHT, out at OFF.

Controls	Location	Function
Panel edge lights 2DS3, 2DS4, 2DS7, and 2DS10.		Light control box front panel (controlled by PANEL switch S3).
CODE SELECT switch assemblies.		Sif codes, in the form of numbers, are set with CODE SELECT switch assemblies and are shown on indicators.
		Numbers are lit by internal lights controlled by PANEL switch 2S3 and selected by MODE SELECT switch 2S6.
MODE 1 switch assemblies 2A3 and 2A4 (two pushbutton switches).		When pressed, change numerals of mode 1 sif code.
MODE 2 switch assemblies 2A5 thru 2A8 (four pushbutton switches).		Same as MODE 1 (except mode 2 code).
MODE 3/A switch assemblies 2A9 thru 2A12 (four pushbutton switches).		Same as MODE 1 (except mode 3/A code).
CHALLENGE lamp 2DS1 (green).		Lights when CHALLENGE switch 2S1 is held to ON (or external challenge enable line is grounded) and system is functioning properly.
PROC SELF TEST fault indicator lamp 2DS8 (red).		When lighted, indicates fault in processor 1A1 (see TM 11–5895–687–35–2).
R/T SELF TEST fault indicator lamp 2DS9 (red).		When lighted, indicates fault in receiver-transmitter 1A3 (see TM 11–5895–687–35–4).
KIR SELF TEST fault indicator lamp 2DS6 (red).		When lighted, indicates fault, no code set in, or that a low randomness condition exists in the interrogator computer.
SYN SELF TEST fault indicator lamp 2DS5 (red).		When lighted, indicates fault in synchronizer 1A2 (see TM 11–5895–687–35–3). *Note:* SELF TEST fault indicator lamps will light if POWER switches on the corresponding assemblies are set to OFF.
CHALLENGE switch 2S1 (three-position spring loaded toggle, center position OFF).		When held to ON, permits IFF set to challenge and receive replies.
		When held to TEST, provides simulated target return pattern to radar ppi scope, which must be specially set up to display test targets.
LAMP TEST switch 2S5 (pushbutton).		When depressed, lights all SELF TEST fault lamps and CHALLENGE indicator lamp.
GTC switch 2S2 (two-position toggle).		When set to ON, enables gain time control circuits, decreasing receiver gain for close-in target replies.
PROCESSOR switch 2S4 (two-position toggle).		When set to IN, processed mode 4 target video or defruited SIF video are displayed in real time on the radar ppi scope; when set to BYPASS, all decoded reply video is displayed directly on radar ppi scope without processing.

Controls	Location	Function
SIF REPLIES switch 2S7 (two-position toggle, spring-loaded to CODED position).		When at CODED, only the selected SIF code and mode replies are displayed on the radar ppi scope. When held at ALL, all sif replies of the selected mode, regardless of code setting, are displayed on the radar ppi scope.
MODE 4 switch 2S8 (four-position rotary) guard pull and rotation required to select ZERO and CODE.		Controls operation in Mode 4.
HOLD positions, which are momentary.		*Switch Position* — *Function* CODE HOLD — Applies a mechanical hold on Mode 4 code setting when power will be removed from computer for more than five seconds. A — Selects Mode 4 code A B — Selects Mode 4 code B ZERO — Removes Mode 4 code setting from interrogator computer.
MODE SELECT switch S26 (six-position, three section rotary) guard pull and rotation required to select TEST 4 and LOCKOUT OVERRIDE positions, which are momentary.		TEST (S6A front) — Provides a mode 4 enable to the interrogator computer and to lamp driver card 2A1. (S6B front) — Special test position which provides a mode 4 test (verification bit 1) enable (ground) to the interrogator computer. (S6B rear) — No function in this position. 1 (S6A front) — Provides a mode 1 enable (ground) to the synchronizer and to lamp driver card 2A1. (S6B front) — Provides a ground to light indicator lamps in switch assemblies A3 and A4. (S6B rear) — ,Provides an sif enable (ground) to lamp driver card 2A1. 2 (S6A front) — Provides a mode 2 enable to the synchronizer and to lamp driver card 2A1. (S6B front) — Provides a ground to light indicator lamps in switch assemblies A5 through A8.

Controls	Location	Function	
		(S6B rear)	Provides an sif enable to lamp driver card 2A1.
		3/a (S6A front)	Provides a mode 3/A enable to the synchronizer and to lamp driver card 2A1.
		(S6B front)	Provides a ground to light indicator lamps in switch assemblies A9 through A12.
		(S6B rear)	Provides an sif enable (ground) to lamp driver card 2A1.
		LOCKOUT OVERRIDE (S6A front)	Provides a mode 4 enable to the interrogator computer and to lamp driver card 2A1.
		(S6B front)	Provides a mode 4 noise alarm override enable to the interrogator computer.
		(S6B rear)	No function in this position.

Section II. CONTROL CIRCUITS TROUBLESHOOTING CHART

7-3. General

a. A symptom troubleshooting procedure is provided to assist in isolating trouble that has been sectionalized to the control circuits. Troubles that have been sectionalized to the control circuits can usually be isolated most rapidly by following a procedure based on symptoms that localize the trouble to a component or to a board within the unit.

b. The symptoms given in paragraph 7–6 consist of indications obtained on the control box and the power control panel. To troubleshoot the control circuits based on symptoms, follow the steps given below.

(1) Observe indications on the control box and the power control panel.

(2) Compare the indications with those listed in the symptoms.

(3) If the indications correspond to those listed in a particular symptom, follow the procedure given in that particular paragraph to isolate the trouble.

NOTE

All inputs to and outputs from the control box except +28 vdc primary power, are either grounds or open circuits. Open circuits as defined herein, have a resistance greater than 90,000 ohms.

7-4. Test Equipment Required to Troubleshoot Control Circuits

A multimeter is the test equipment required to troubleshoot the control circuits.

7-5. Preparation of Control Circuits for Troubleshooting

To prepare the IFF set for troubleshooting it is necessary to use the hot mockup configuration with a known good processor, synchronizer, receiver-transmitter and interrogator computer. The front panel of the control box is to be removed to provide access to switch contacts, lamp driver board 2A1 and remote error indicator board 2A2. The power control panel on the interrogator group case is to be removed to provide access to switch relay, and line filter contacts.

a. Set up the IFF set in the mockup configuration as shown in figure 10–1.

b. Remove the front panel of the control box using the procedures in TM 11–5895–687–12, paragraph 5–18 *a* (1) and (2).

c. Remove the power control panel by loosening six captive screws (TM 11–5895–687–12, fig. 3–2) and swinging power control panel forward; be careful not to damage the wiring harness.

7-6. Control Circuits Symptom Troubleshooting Chart

Symptom	Probable cause	Corrective measures
POWER indicator lamp 1DS1 does not light when pressed.	POWER lamp 1DS1, capacitor 1C1 line filter FL5 or wiring is deflective.	Check lamp 1DS1. *a.* If lamp 1DS1 is good, check for +28 v at pins 1 and 3 of line filter FL5. (1) If +28 v is present at pin 1, but not at pin 3, line filter 1FL5 is defective. (2) If +28 v is not present at pin 1, check capacitor 1C1, and check wiring for continuity.
POWER indicator lamps 1DS1 and 2DS2 do not light and TOTAL HOURS meter 1M1 does not operate when POWER circuit breakers 1CB1 and 2CB1 are set to ON.	POWER circuit breaker 1CB1 and 2CB1, power reply 1K1, associated line filter or wiring defective.	Press LAMP TEST switch 2S5. *a.* If POWER lamp 2DS2 lights, check power relay 1K1 for +28 v at contacts X1 and A2, check line filter 1FL1–A1 and 1FL1–A2, and wiring for continuity. *b.* If POWER lamp 2DS2 does not light, check for +28 v at input and output terminals of POWER circuit breakers 1CB1 and 2CB1, and check line filter 1FL1–A3 and wiring for continuity.
Panel edge lighting goes out when PANEL switch 2S3 is set from BRIGHT to DIM.	PANEL switch 2S3 defective, resistor 2A2R6 open, or wiring defective.	Check switch 2S3 for open contact, resistor 2A2R6 for proper value, and wiring for continuity.
CODE SELECT switch assembly lamps go out when PANEL switch 2S3 is set from BRIGHT to DIM.	PANEL switch 2S3 defective, resistor 2A2R5 open, or wiring defective.	Check switch 2S3 for open contact, resistor 2A2R5 for proper value, and wiring for continuity.
Lamps in CODE SELECT switch assemblies A3 and A4 (MODE 1) are more brightly lighted than are MODE 2 and MODE 3/A switch assembly lamps.	Shunt resistor 2A2R4 open or wiring defective.	Check shunt resistor 2A2R4 for proper value and wiring for continuity.
TOTAL HOURS meter 1M1 does not operate but POWER indicator lamp 1DS1 is lighted.	TOTAL HOURS meter 1M1 or wiring is defective.	Check TOTAL HOURS meter and wiring for continuity.
SELF TEST fault indicator lamps do not light when a malfunction exists in either the receiver-transmitter, synchronizer, processor, or interrogator computer, as indicated by a lighted fault lamp on any of the first three, but SELF TEST fault indicator lamps light when LAMP TEST switch 2S5 is pressed.	Lamp driver board 2A1 associated line filter, or wiring is defective.	Replace defective lamp driver board 2A1 or check line filters 1FL3–C3 and 1FL3–C4 for KIR, 1FL1–B1 for RIT, 1FL1–C1 for SYN, and 1FL1–B2 for PROC and wiring for continuity.

Symptom	Probable cause	Corrective measures
SELF TEST fault indicator lamps do not light and POWER lamp 2DS2 goes off when LAMP TEST switch 2S5 is pressed.	LAMP TEST switch 2S5 or wiring is defective.	Check continuity of LAMP TEST switch 2S5 and wiring.
POWER lamp 2DS2 remains lit but SELF TEST fault indicator lamps do not light when LAMP TEST switch 2S5 is pressed.	Lamp driver board 2A1 is defective.	Replace lamp driver board 2A1.
One of the selected modes (mode 1, mode 2, or mode 3/A) is not correctly enabled.	1. An associated CODE select switch or diodes CR1, CR2 or CR3 of that switch.	1. Check diodes CR1, CR2 and CR3. Check CODE SELECT switch assembly by pressing the pushbutton a predetermined number of times and while holding CHALLENGE switch 2S1 to ON, checking the cathodes of diodes CR1, CR2, and CR3 consecutively to determine if binary code is correct. An octal one is represented by a ground at diode CR1 and open circuits at diodes CR2 and CR3. Refer to the following for the binary representation of the octal code numbers 0 through 7.

	Binary number		
Code number	2^2 *CR3*	2^1 *CR2*	2^0 *CR1*
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0

1 = ground
0 = open circuit

	2. An associated part of line filter 1FL2 or wiring defective.	2. Check associated line filter and wiring for continuity.
IFF set does not challenge when CHALLENGE switch 2S1 is set to ON, and no SELF TEST fault lamps on control box light.	CHALLENGE switch 2S1 or wiring is defective.	Check for a ground level at pin J1–X when CHALLENGE switch 2S1 is held at ON. If indication is abnormal, either switch or wiring is defective.
IFF set does not challenge in one mode, but challenges in all other modes.	MODE SELECT switch S6A, associated line filter, or wiring defective.	Check MODE SELECT switch S6A, line filter 1FL1–C4 for mode 1, 1FL–C3 for mode 2, 1FL1–C2 for mode 3/A, or 1FL3–A4 and 1FL4–B3 for mode 4, or wiring for continuity.
IFF set does not challenge with MODE SELECT switch 2S6 set to TEST 4, but challenges in all other positions.	MODE SELECT switch 2S6B, associated line filters, or wiring defective.	Check MODE SELECT switch 2S6B front line filters 1FL3–B2 or 1FL4–C1, or wiring for continuity.
IFF set does not challenge with MODE SELECT switch 2S6 set to LOCKOUT-OVERRIDE, but challenges in all other positions.	MODE SELECT switch 2S6B, associated line filters, or wiring defective.	Check MODE SELECT switch 2S6B front, line filters 1FL3–B1 or 1FL3–B1 or 1FL4–B2, or wiring for continuity.
Remote error indicator is not enabled when one of the SELF TEST lamps is lighted, but is enabled when any other fault lamp is lighted.	Associated diode CR1, CR2, CR3 or CR4 on error indicator card 2A2.	Check diode CR1 if PROC SELF TEST lamp is lighted, CR2 for KIR, CR3 for R/T and CR4 for SYN.

Symptom	Probable cause	Corrective measures
Remote error indicator is not enabled when any self test lamp is lighted.	Lamp driver card 2A1, or wiring defective. 2. Error relay driver 2A2Q1, diode 2A2CR5 or 2A2CR6, error relay 2A2K1, or wiring defective.	1. Check for +28 v at terminal 16 on remote error indicator card 2A2. If +28 v is not present replace lamp driver card 2A1. 2. Check transistor 2A2Q1, diodes 2A2CR5 and CR6, and wiring for continuity.
Mode 4 code zeroizes when power is applied to the interrogator computer.	MODE 4 switch 2S8, code zeroize relay 1K2, associated line filter or wiring defective.	Check MODE 4 switch S8A rear, contact 4, line filters 1FL3–C2 and 1FL4–C3 and associated wiring for short to ground. Check code zeroize relay 1K2 for open circuit on contact A2.
Mode 4 code zeroizes when MODE 4 switch 2S8 is set to CODE HOLD and power is removed from the interrogator computer.	MODE 4 switch 2S8, associated line filter, or wiring defective.	Check MODE 4 switch S8A front contact 12, 2S8A rear contact 1, line filters 1FL3–B3, 1FL4–B1, 1FL3–C1, and 1FL4–C4 and wiring for continuity.
Gtc circuits are not enabled when GTC switch 2S2 is set to ON.	GTC switch 2S2, line filter 1FL1–A4, or wiring defective.	Check GTC switch 2S2, line filter 1FL1–A4, and wiring for continuity.
Processor is not bypassed when PROCESSOR switch 2S4 is set to BYPASS.	PROCESSOR switch 2S4, line filter. 1FL2–C3, or wiring defective.	Check PROCESSOR switch 2S2, line filter 1FL2–C3, and wiring for continuity.
Bracket decoding circuits are not enabled when SIF REPLIES switch 2S7 is set to ALL.	SIF REPLIES switch 2S7, line filter 1FL3–A1, or wiring defective.	Check SIF REPLIES switch 2S7, line filter 1FL3–A1 and wiring for continuity.
The interrogator computer does not receive primary power when power relay 1K1 is energized.	Line filter 1FL4–B4 or wiring defective.	Check line filter 1FL4–B4 and wiring for continuity.

Section III. TESTING THE CONTROL CIRCUITS

7-7. General

This section describes the testing procedures required to check the control circuits of the interrogator set. Bench testing of the interrogator group case is described in paragraph 7–11, and bench testing of the control box is described in paragraph 7–16. Testing of the complete interrogator set is described in paragraph 7–9.

7-8. Test Equipment Required

No test equipment is required for these tests.

7-9. Testing Procedure

To test the control circuits of the IFF set, perform the procedures as described in the troubleshooting based on starting procedure chart (para 6–5). The indications, as described in the *Normal indications* column of this chart will indicate satisfactory operation of the control circuits.

Section IV. TROUBLESHOOTING AND REPAIR OF CABINET, INTERROGATOR SET GROUP CY-6442/TPX–50

7-10. General

Bench servicing of the interrogator group case is accomplished in a complete hot mockup configuration and is performed when it is known that the interrogator group case is defective or when it has been repaired.

7-11. Interrogator Group Case Bench Servicing Connections

To prepare the interrogator group case for bench servicing, proceed as follows:

a. Check the interrogator group case for shorts using the resistance chart paragraph 5–7.

b. Using Test Facilities Set AN/TPM–24(V)3, connect the equipment as shown in figure 5–2 and described in paragraph 5–25. Extend assemblies only if necessary.

7-12. Interrogator Group Case Bench Troubleshooting

a. Bench troubleshooting of the interrogator group case is contained in the symptom troubleshooting chart (para 7–6). This chart covers all active components of the interrogator group case.

b. If it is suspected that the wiring of the interrogator group case is faulty, refer to figure 12–5 and make continuity checks for all wires.

7-13. Removal and Replacement of Parts of Interrogator Group Case

To gain access to the majority of the active components of the interrogator group case it is necessary to remove the power control panel (*a* below). After removal of the power control panel, in order to gain access to both sides of line filters FL1 through FL4 it is necessary to remove the filter panel (*b*, below). To gain access to the internal portions of connectors 1J5 through 1J8 it is necessary to remove the connector panel located on the rear of the interrogator group case (*c* below). To gain access to the internally mounted connectors, for the assemblies in the interrogator group case, and to resistors 1R2 and 1R3 it is necessary to remove the two case panel from the rear of the interrogator group case (*d* below). For removal and replacement of individual piece parts refer to paragraph 5–14.

a. Removal and Replacement of Power Control Panel.

(1) To remove the power control panel, loosen six captive screws (fig. 6–1) and swing the panel out from the interrogator group case. Be careful not to damage connecting cabling.

(2) To replace the power control panel, swing the panel into position on the interrogator group case and secure with six captive screws.

b. Removal and Replacement of Filter Panel.

(1) To remove the filter panel, remove 8 retaining screws (fig. 7–1) which secure it to its housing. Move the panel forward, while being careful not to damage connecting wires, until the rear of the panel is exposed.

(2) Replace the filter panel by placing it in position on its housing and while ensuring that grounding gasket is in position, securing it with eight retaining screws.

c. Removal and Replacement of Connector Panel.

(1) Remove the connector panel by removing six retaining screws and moving the panel out from the group case until the interior portion of the panel is exposed (fig. 7–2). Be careful not to damage connecting wires.

(2) Replace the connector panel by placing it in position on the interrogator group case and, while ensuring that gasket is in position, securing it with six retaining screws.

d. Removal and Replacement of Case Panels.

(1) To remove the case panels from the rear of the interrogator group case, remove 10 retaining screws from the upper panel and 16 retaining screws from the lower panel. Remove panels (fig. 7–3).

(2) To replace the case panels, place them in position on the interrogator group case and, while insuring that the gaskets are in position, securing the upper panel with 10 retaining screws and the lower panel with 16 retaining screws.

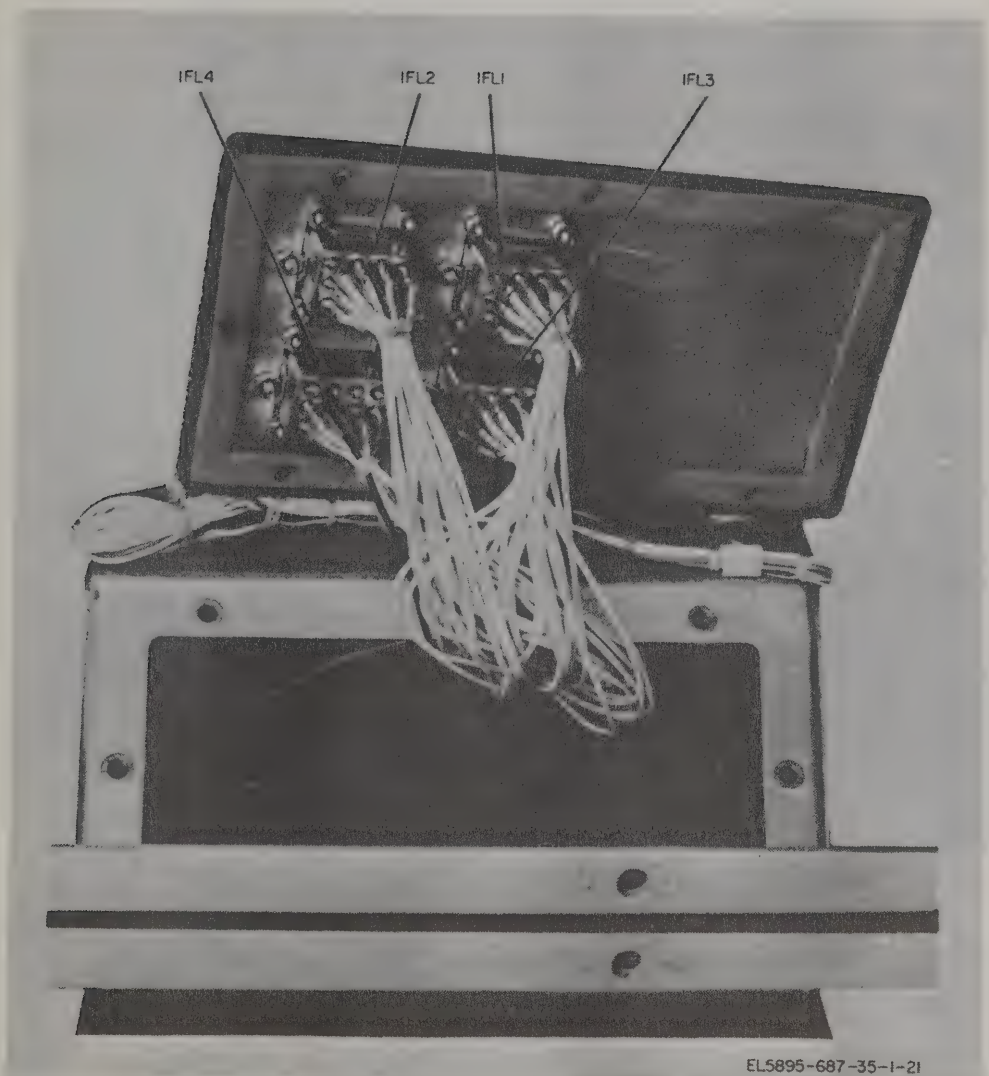


Figure 7–1. Filter panel, inside view.

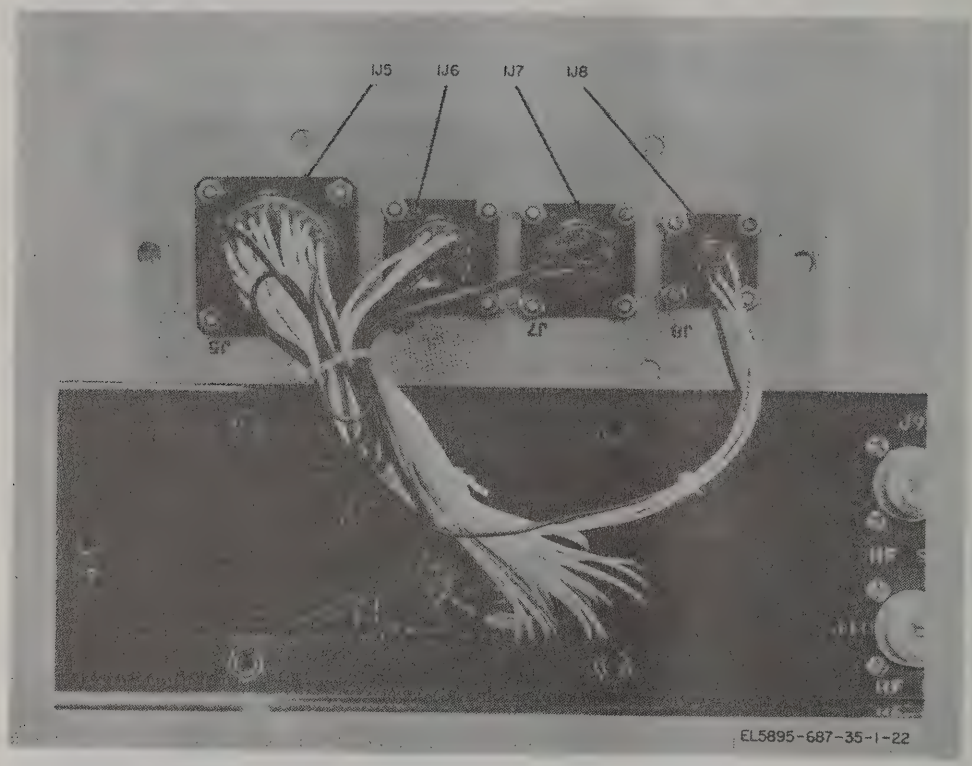


Figure 7–2. Connector panel, inside view.

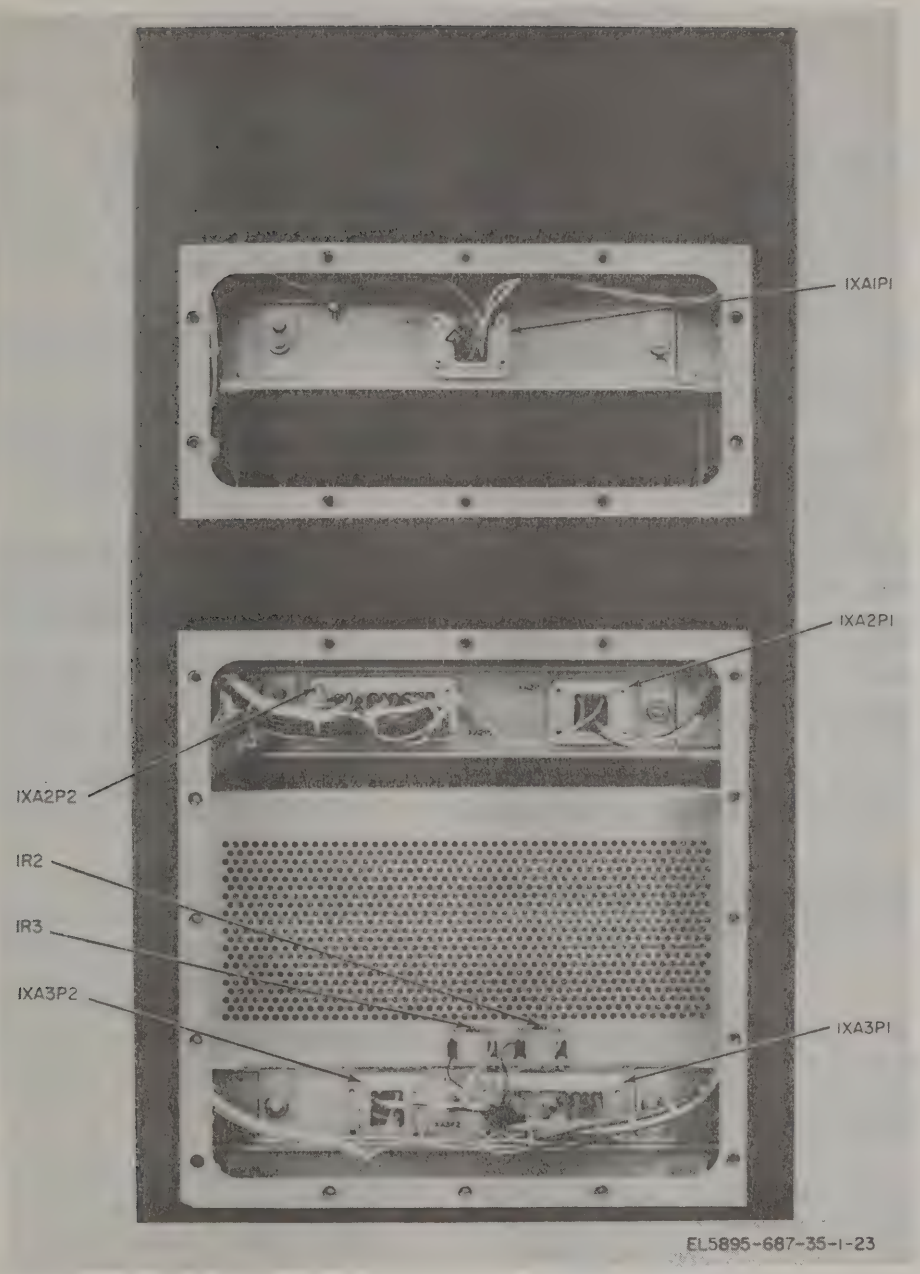


Figure 7-8. Interrogator group case, rear view, panels removed.

Section V. TROUBLESHOOTING AND REPAIR OF CONTROL, INTERROGATOR SET C-7651/TPX-50

7-14. General

Bench servicing of the control box is accomplished in a complete hot mockup configuration and is performed when it is known that the control box is defective or when it has been repaired.

7-15. Control Box Bench Servicing Connections

To prepare the control box for bench servicing, proceed as follows:

a. Check the control box for shorts using the resistance chart in paragraph 5-8.

b. Using Test Facilities Set AN/TPM-24(V)3, connect the equipment as shown in figure 5-3 and described in paragraph 5-25. Extend assemblies only if necessary.

7-16. Control Box Bench Troubleshooting

Bench troubleshooting on the control box is contained in the symptom troubleshooting chart (para 7-6). This chart covers with exception of lamp driver card 2A1, all active components of the control box.

7-17. Removal and Replacement of Parts of Control Box

a. Removal and replacement of parts in the control box are described in paragraphs 5-18 and 5-19, TM 11-5895-687-12.

7-18. Removal and Replacement of Parts on Lamp Driver Card 2A1 and Remote Error Indicator Card 2A2

Removal and replacements procedures, as parts as applicable to lamp driver card 2A1 and remote indicator card 2A2, are contained in paragraphs 5-14 and 5-15.

CHAPTER 8

LAMP DRIVER CARD 2A1 TROUBLESHOOTING AND REPAIR

8-1. Reference Data

The following information will be helpful when troubleshooting or repairing lamp driver card 2A1, which contains no operating controls.

Reference	*Data*
Figure 12–7	Lamp driver card 2A1, schematic diagram and component locations.
Figure 12–4	Control circuits, functional block diagram.

8-2. Lamp Driver Card 2A1 Troubleshooting

a. A symptom troubleshooting procedure is provided to assist in isolating trouble that has been localized to the lamp driver card in the control circuits. Troubles that have been traced to the lamp driver card can usually be isolated most rapidly by following a procedure based on symptoms that localize the trouble to a component.

b. The symptoms given in paragraph 8–5 consist of indications obtained on the control box. To troubleshoot the lamp driver card based on symptoms, follow the steps given below.

(1) Observe indications obtained on the control box and other assemblies.

(2) Compare the indications obtained with those listed in the symptoms.

(3) If the indications obtained correspond to those listed in a particular symptom, follow the procedure given in that particular subparagraph to isolate the trouble.

8-3. Test Equipment Required

A multimeter is the test equipment required to troubleshoot lamp driver card 2A1.

8-4. Preparation of Lamp Driver Card 2A1 for Troubleshooting (fig. 8–1)

a. To gain access to the test block points for voltage measurements, follow the procedures in TM 11–5895–687–12, paragraphs 5–14*b* and 5–18*a* (1), (2), and (3), and figure 8–1.

8-5. Lamp Driver Card 2A1 Symtom Troubleshooting Chart (fig. 12–7)

Symptom	Probable cause	Corrective measures
Notes: 1. Chart is based on assumption that challenging is taking place normally. 2. Parts listed without unit designation prefix are on a lamp driver card 2A1; for example, R13 is on lamp driver card, but 2S5 is on control box, unit 2.		
POWER circuit breaker 2CB1 trips when set to ON.	Shorted capacitor C1.	Check capacitor C1 and replace if defective.

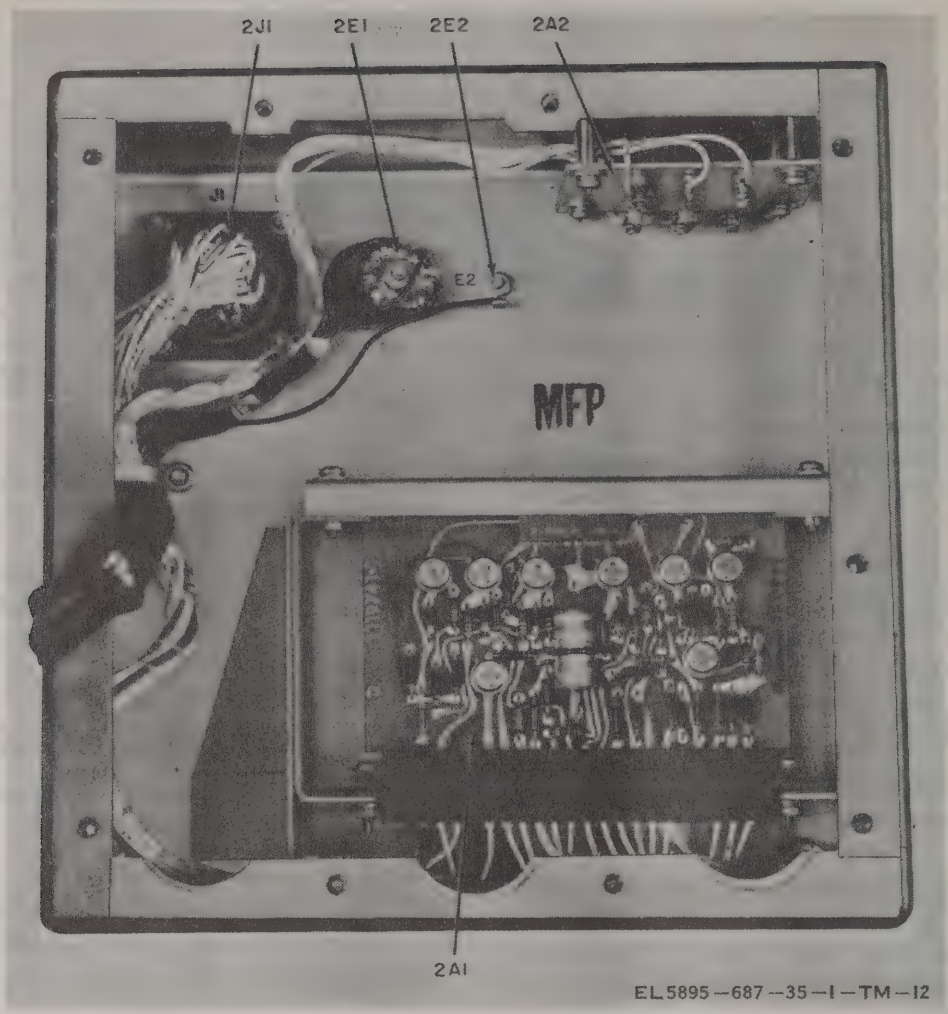


Figure 8–1. Lamp driver card 2A1.

Symptom	Probable cause	Corrective measures
CHALLENGE lamp and SELF TEST fault lamps do not light when they should, but pressing LAMP TEST switch 2S5 lights all lamps.	No +28 vdc power being distributed to lamp drivers.	Check diode CR1 and replace if defective.
When LAMP TEST pushbutton 2S5 is pressed, one or more of CHALLENGE and SELF TEST lamps do not light.	Faulty diode associated with unlighted lamp.	Check diode associated with lamp that does not light: CR3 through CR7.
While challenging in one of the 4 possible modes, neither CHALLENGE lamp 2 DS1 nor any of the SELF TEST fault lamps on the control box lights.	1. Defective diode associated with mode enable line being used.	1. Move MODE SELECT switch 2S6 successively through 3 remaining modes. If symptom persists, proceed to probable cause below. If CHALLENGE lamp lights, check diode associated with original challenge mode and replace: CR16 for Mode 1 CR17 for Mode 2 CR18 for Mode 3/A CR19 for Mode 4

Symptom	Probable cause	Corrective measures
	2. Challenge lamp driver circuit defective.	2. Check transistors Q1 and Q2, and associated circuitry as follows:
SELF TEST fault lamp on control box does not light when a malfunction exists in synchronizer, processor, or receiver-transmitter, as indicated by a lighted FAULT lamp on the affected assembly, but SELF TEST fault lamp lights when LAMP TEST switch 2S5 is pressed.	Defective fault indicator enable lamp driver circuit.	Check lamp driver transistor and associated circuitry as follows: For synchronizer: Q3 For processor: Q6 For receiver-transmitter: Q4 For interrogator computer, which has no fault lamps: Q7
SYN SELF TEST fault lamp and CHALLENGE lamp both light.	1. Faulty challenge lamp driver circuit.	1. Move CHALLENGE switch 2S1 to OFF. If symptom persists, check diode CR15 transistors Q1 and Q2, and associated circuitry. If CHALLENGE lamp goes off, proceed to probable cause 2, below.
	2. Faulty diode CR14 or CR8.	2. Replace diode.
PROC SELF TEST fault lamp lights, with PROCESSOR switch 2S4 in BYPASS position, but CHALLENGE lamp remains off.	1. Processor bypass enable line open.	1. Check for continuity.
	2. Diode CR11 faulty.	2. Check diode CR11 and replace.
PROC SELF TEST fault lamp lights with PROCESSOR switch 2S4 in IN position, but CHALLENGE lamp lights.	1. Faulty resistor R15 or diode CR12.	2. Check and replace faulty component.
	2. Challenge lamp driver circuit defective.	2. Check diode CR8, transistors Q1 and Q2.
KIR SELF TEST fault lamp lights, with MODE SELECT switch 2S6 in 1, 2, or 3/A position, but CHALLENGE lamp remains off.	1. Diode CR9 faulty.	1. Check diode CR9.
	2. Defective diode associated with mode in which challenging is taking place.	2. Move MODE SELECT switch 2S6 successively to 2 remaining sif modes. If symptom is the same, proceed to step 4, below. IF CHALLENGE lamp lights, check diode associated with original challenge mode: CR16 for Mode 1 CR17 for Mode 2 CR18 for Mode 3/A
	3. Challenge lamp driver circuit defective.	3. Check transistors Q1 and Q2, and associated circuitry.
KIR SELF TEST fault lamp lights, with MODE SELECT switch 2S6 in mode 4 position, but CHALLENGE lamp lights.	1. Faulty resistor R14 or diode CR10.	1. Check and replace faulty component.
	2. Challenge lamp driver circuit defective.	2. Check diode CR8, transistors Q1 and Q2, and associated circuity.
R/T SELF TEST lamp is on, the RF SWITCH FAULT lamp on the receiver-transmitter is off (signifying no rf switch fault), but CHALLENGE lamp is on.	1. Isls pulse inhibit circuit faulty (output should be high to junction of R8 and CR13).	1. Check inverter Q5 and associated circuitry (resistor R8 and diode CR13).
	2. Challenge lamp driver circuit defective.	2. Check diode CR8, transistors Q1 and Q2, and associated circuitry.

8-6. Voltage and Resistance Measurement

a. General. Voltage and resistance measurements are an aid in determining circuit conditions and evaluating clues in the course of trouble-shooting. Carefully read the notes on the voltage and resistance charts and exactly duplicate the conditions under which the normal readings were obtained.

b. Measurement conditions. All voltage and resistance readings were taken with respect to ground (J1–7). The dc voltage readings are taken at the test block points listed, on a normally operating card with LAMP TEST switch depressed and were read on the 50V scale of the multimeter. Resistance readings on the etched connector are taken on a normally operating card that has been removed from the control box and were read on the R X 10,000 scale of the multimeter.

c. Transistor Testing. See chapter 5 for information on out-of-circuit characteristics for the transistors used on lamp driver card 2A1.

Terminal	*Voltage (dc)*	*Resistance in ohms* *Forward*	*Reverse*
Test Point J1–1	25.5	26K	19K
Test Point J1–2	25.5	27K	19K
Test Point J1–3	Not Used	INF	INF
Test Point J1–4	Not Used	INF	INF
Test Point J1–5	25.5	30K	19K
Test Point J1–6	26	24K	19K
Test Point J1–7	GRD	0	0
Test Point J1–8	Not Used	INF	INF
Test Point J1–9	25.5	30K	19K
Test Point J1–10	25.5	INF	19K

Terminal	*Voltage (dc)*	*Resistance in ohms* *Forward*	*Reverse*
ETCHED CONNECTOR PIN NO.			
1	–	INF	INF
2	–	INF	INF
3	–	30K	INF
4	–	INF	INF
5	–	INF	INF
6	–	45K	41K
7	–	25K	20K
8	–	INF	INF
9	–	22K	19K
10	–	INF	INF
11	–	INF	INF
12	–	16K	66K
13	–	INF	INF
14	–	25K	20K
15	–	INF	INF
16	–	45K	42K
17	–	INF	50K
18	–	INF	50K
19	–	INF	INF
20	–	28K	20K
21	–	0	0
22	–	44K	40K
23	–	0	0
24	–	50K	40K
25	–	INF	INF
26	–	33K	20K
27	–	INF	50K
28	–	INF	50K
29	–	13K	13K
30	–	13K	13K
31	–	33K	23K
32	–	INF	20K
33	–	27K	38K
34	–	INF	50K
35	–	INF	INF
36	–	INF	INF
37	–	INF	INF
38	–	43K	25K
39	–	INF	INF
40	–	INF	50K
41	–	INF	INF
42	–	INF	50K
43	–	INF	50K
44	–	INF	50K

CHAPTER 9

COMPLETE ALIGNMENT AND TESTING OF AN/TPX-50

9-1. General

a. This chapter covers all the adjustments, alignments, and testing to be accomplished in the IFF set. Adjustment, alignment, and testing is accomplished on an individual basis in each assembly of the IFF set: synchronizer, receiver-transmitter, and processor. No adjustment or alignment is required in the control box or interrogator group case.

b. After the assemblies have been individually aligned, adjusted, and tested, as described in each of their equipment manuals (para 1–3*j*), no further adjustment or alignment is necessary when they are interconnected into the IFF system.

9-2. Adjustment and Alignment Procedures

The following chart lists the adjustment and alignment procedures that should be performed to completely align the IFF set. Step-by-step directions for performing the procedures listed in the *Adjustment or alignment* column are contained in the manual and paragraph listed in the *Procedure* column. Perform the procedures in the order listed below.

Alignment or adjustment	*Procedure*
Processor	TM 11–5895–687–35–2
+5-volt adjustment	Para 19–10
Monitor meter calibration	Para 19–11
16-megacycle oscillator symmetry adjustment	Para 14–10
Reply lockout multivibrator adjustments	Paras 16–10 and 16–11
Synchronizer	TM 11–5895–687–35–3
+12-Volt adjustment	Paras 18–10 and 18–11
+5-Volt adjustment	Paras 18–10 and 18–12
Sif challenge video pulse width adjustment	Paras 14–10 and 14–11
Mode 4 challenge video pulse width adjustment	Paras 14–10 and 14–12
Receiver video threshold adjustment	Paras 15–10 and 15–11
Display gate width adjustment	Paras 16–10 and 16–11
IFF display video adjustment	Paras 16–10 and 16–12
Receiver-transmitter	TM 11–5895–687–35–4
Power supply circuit adjustment	Para 14–14
Diplexer Filter adjustment	Para 12–24
Receiver preselector alignment	Para 12–15
Local oscillator/exciter adjustment	Para 12–16
Exciter frequency multiplier alignment	Para 12–17
Receiver local oscillator coupling adjustment	Para 12–18
IF logarithmic detector adjustment	Para 12–19
Receiver gate adjustment	Para 12–20
Gtc adjustment	Para 12–21
Video Processor, baseline clipping adjustment	Para 12–22
Rsls comparator adjustment	Para 12–23
Self-test signal generator card adjustment	Para 13–14
Self-test circuit adjustment	Para 13–15
Challenge Monitor adjustment	Para 11–15

9-3. Test Procedures

The following chart lists the testing procedures that should be performed to completely test the IFF set. Step-by-step directions for performing the procedures listed in the *Test* column, can be found in the manual and paragraph listed in the *Procedure* column.

Test	*Procedure*
Processor	TM 11–5895–687–35–2
Power supply system test	Para 19–14
Timing system test	Para 14–13
Memory system test	Para 15–10
Target arithmetic system test	Para 16–14

Test	*Procedure*
Friend arithmetic system test	Para 17–10
Self-test system test	Para 18–15
Synchronizer	TM 11–5895–687–35–3
Power supply and power distribution circuit test	Paras 18–14 and 18–15
Timing circuit test	Paras 13–8 and 13–9
Challenge encoding circuit test	Paras 14–14 and 14–15
Reply decoding circuit test	Paras 15–13 and 15–14
Display video interface circuit test	Paras 16–14 and 16–15
Fault indication circuit test	Paras 17–8 and 17–9
Receiver-Transmitter	TM 11–5895–687–35–4
Power supply circuit test	Para 14–17
Decoding sensitivity, bandwidth, recovery time, rsls, and gtc tests	Para 12–27
Video output tests	Para 12–28
Operating frequency test	Para 11–19
Sum and difference channel power output and pulse characteristics test	Para 11–18
Sum channel pulse train droop test	Para 11–20
Challenge monitor test	Para 11–21
Transponder suppression test	Para 11–22
Self-test circuit tests	Para 13–18

CHAPTER 10

GENERAL SUPPORT TESTING PROCEDURES

All information in chapter 10, including figure 10-1, is deleted.

CHAPTER 11

DEPOT OVERHAUL STANDARDS

11-1. Applicability of Depot Overhaul Standards

Interrogator Set AN/TPX–50 (hereafter referred to as the IFF set) must be tested thoroughly after rebuild or repair to insure that it meets adequate performance standards for return to stock and reissue. First use the separate test procedures listed below to measure the performance of the three IFF set assemblies covered by separate DS, GS and depot maintenance manuals. Then, with those assemblies known to be satisfactory, use the test procedures given in this chapter to measure the performance of the remaining rebuilt or overhauled assemblies as parts of the complete rebuilt or overhauled IFF set. It is mandatory that each complete IFF set to be reissued, or returned to stock for reissue, meet all of the performance standards given in this chapter and in the separate depot overhaul standards chapters listed in the following chart.

NOTE

Cable Assembly, Special Purpose, Electrical CX–10876/TPX–50 (7' 8") (hereafter referred to as cable W1) and Cable Assembly, Special Purpose, Electrical, Branched CX–10878/TPX–50 (6') (hereafter referred to as cable W2) are supplied with but are not part of the IFF set.

Assembly	*Common name*	*Location of depot overhaul standards*
Signal Processor CP–936/TPX–50	Processor	Chapter 24 of TM 11–5895–687–35–2
Electrical Synchronizer SN–421/TPX–50	Synchronizer	Chapter 23 of TM 11–5895–687–35–3
Radio Receiver Transmitter RT–903/TPX–50	Receiver-Transmitter	Chapter 19 of TM 11–5895–687–35–4
Interrogator Set Group Cabinet CY–6442/TPX–50	Interrogator group case	This chapter
Interrogator Set Control C–7651/TPX–50	Control box	This chapter

11-2. Applicable References

a. Repair Standards. Applicable procedures of the Signal Corps depot performing this test, and its general standards for repaired signal equipment, form a part of the requirements for testing this equipment.

b. Technical Publications. The following technical publications are applicable to this equipment:

Equipment and subject	*Publication*
Operator and Organizational Maintenance: Interrogator Set AN/TPX–50	TM 11–5895–687–12
Organizational Maintenance Repair Parts and Special Tools List: Interrogator Set AN/TPX–50.	TM 11–5895–687–20P

Equipment and subject	*Publication*
DS, GS, and Depot Maintenance Repair Parts and Special Tools List: Interrogator Set AN/TPX–50.	TM 11–5895–687–35P–1
DS, GS, and Depot Maintenance: Signal Processor CP–936/TPX–50.	TM 11–5895–687–35–2
DS, GS, and Depot Maintenance Repair Parts and Special Tools List: Signal Processor CP–936/TPX–50.	TM 11–5895–687–35P–2
DS, GS, and Depot Maintenance: Synchronizer, Electrical SN–421/TPX–50.	TM 11–5895–687–35–3
DS, GS, and Depot Maintenance Repair Parts and Special Tools List: Synchronizer Electrical SN–421/TPX–50.	TM 11–5895–687–35P–3
DS, GS, and Depot Maintenance: Receiver-Transmitter, Radio RT–903/TPX–50.	TM 11–5895–687–35–4
DS, GS, and Depot Maintenance Repair Parts and Special Tools List: Receiver-Transmitter, Radio RT–903/TPX–50.	TM 11–5895–687–35P–4

c. Modification Work Orders. Perform all applicable modification work orders (MWO's) pertaining to this equipment before making the tests specified. DA Pam 310–7 lists all applicable MWO's.

11-3. Test Facilities Required

The following equipments, or suitable equivalents, will be employed in determining compliance with this specific standard.

a. Test Equipment.

Equipment	*Qty reqd*	*Common name*	*Applicable literature*
Counter, Electronic, Digital Readout AN/USM–207A	1	Counter	NAVSHIPS 0969-125-0010 NAVSHIPS 0969-125-0020
Multimeter AN/PSM–6B	1	Multimeter	TM 11–6625–475–10
Oscilloscope AN/USM–281A	1	Oscilloscope	TM 11–6625–1703–15
Power Supply PP–2953A/U	1	28–volt dc power supply.	TM 11–6130–233–12
Radar Test Set AN/UPM–98A.	1	Radar test set.	TM 11–6625–403–15
Simulator, Test Set AN/APM–245A	1	Mode 4 word generator.	TM 11–6625–1711–15–1
Test Facilities Set AN/TPM–24 (V)3.	1	Test facilities set.	TM 11–6625–2398–15–3

b. Additional Equipment. For tests requiring connections to specified pins of W2P1 and of EXTERNAL CHALLENGE receptacle 1J8, the following parts will be helpful if available. If these parts are not available, use care when probing the pins of W2P1 and 1J8 to avoid damaging the pins.

(1) A connector, Amphenol 94–622 or equivalent, to mate with W2P1, and a terminal block with at least 14 terminals, Cinch-Jones Series 500 or equivalent, wired to the connector so that each of the following 14 pins of W2P1 is accessible on a separate terminal:

Pin	*Signal*
W2P1–9	Mode 4 code A/B selection
W2P1–12	Internal jumper, W2P1–12 to W2P1–13
W2P1–13	Internal jumper, W2P1–13 to W2P1–12
W2P1–14	KIR fault indicator enable
W2P1–19	Mode 4 test enable (verification bit 1)
W2P1–20	Chassis ground
W2P1–23	Mode 4 noise alarm override
W2P1–24	Verification bit 2
W2P1–26	Mode 4 enable (challenge control)
W2P1–31	Primary power (+28 vdc)
W2P1–32	Landing gear interlock
W2P1–33	Zeroize return
W2P1–34	System ground
W2P1-37	Refuel hold enable

(2) A connector, MS3116A–10–6P, to mate with EXTERNAL CHALLENGE receptacle 1J8, and a terminal block with at least four terminals, Cinch-Jones Series 500 or equivalent, wired to the connector so that each of the following four pins of 1J8 is accessible on a separate terminal:

Pin	*Signal*
1J8–A	External challenge enable
1J8–B	Remote error indicator enable return
1J8–C	System ground (external challenge enable return)
1J8–E	Remote error indicator enable

11-4. General Test Requirements (fig. 5–3)

a. Test Connections. Perform the tests of paragraphs 11–5 through 11–10 with the IFF set and test equipment connected as shown in figure 5–3. To simplify the setup procedures for the successive tests, connect all test equipment initially as shown by unbroken lines in figure 5–3, and then make additional connections or modifications as directed in the individual test procedures. When one or more of the test equipments shown in figure 5–3 is not included in the list of test equipment required for a test, the corresponding connections shown in figure 5–3 are unnecessary but need not be removed; merely disregard them.

b. Applying Test Equipment Power. Connect the test equipments which require power to a source of 115 volts, 60 cps ac. Then turn on the test equipments, observing the following precautions:

(1) Before turning on the 28–volt dc power supply (used in all tests) for the first time, set the POWER circuit breakers on the control box and interrogator group case power control panel to OFF. Then turn on the 28–volt dc power supply and adjust its output to 28 volts. This will ensure that the power supply voltage is initially within specified limits when the POWER circuit breakers are set to ON.

(2) Before turning on the mode 4 word generator (used only in the mode 4 tests of paragraphs 11–8 and 11–9) for the first time, set the mode 4 word generator TEST WORD AM. control to its midposition or lower (more counterclockwise than midposition). This will insure against excessive TEST WORD pulse amplitude at the synchronizer when the mode 4 word generator is externally triggered (by the EXT TRIG connection shown as a broken line in figure 5–3) and W48AT1 and W48P1 of the test facilities set are connected to the TEST WORD receptacle of the mode 4 word generator.

(3) After turning on all test equipment, allow a warmup period of at least 20 minutes before proceeding with any tests other than the power and indicator test of paragraph 11–5. That test is not affected by warmup drift in the test equipment, and may be performed during the 20–minute warmup period.

c. Initial IFF Set Control Settings. With the POWER circuit breaker on the control box at OFF, set the remaining IFF set controls as follows:

(1) On the control box, set the following switches to the indicated positions:

CODE SELECT – MODE 1	73
– MODE 2	7777
– MODE 3/A	7777
CHALLENGE	OFF (released)
GTC	OFF
PANEL	OFF
PROCESSOR	IN
MODE SELECT	1
SIF REPLIES	CODED (released)
MODE 4	A

(2) On the interrogator group case power control panel, set the POWER circuit breaker to ON.

(3) On the processor, set the POWER circuit breaker to ON and the METER switch to OUT.

(4) On the synchronizer, set the POWER circuit breaker to ON and the meter switch to OUT.

(5) On the receiver-transmitter, set the POWER circuit breaker to ON, the RF PWR SWITCH to HI, and the (internal) XMTR MOD switch to ON.

d. Test Signals Required. Prepare the test equipment to provide the required test signals as directed in (1) through (7) below. When changes must be made during individual tests, make the changes as directed in the corresponding test procedures.

(1) Adjust the radar test set to provide a "0" TRIGGER output (simulated radar triggers) at a prf of 375 pps as follows:

(*a*) On the radar test set CAL–CONTROL panel, set METER SELECT to 500 PRF, and TRIGGER to INT.

(*b*) On the radar test set XTAL MARK & SYNC panel, set SYNC SELECT to INT, and adjust PRF for a reading of 375 (pps) on CAL–CONTROL panel meter.

(2) Adjust the radar test set to provide a simulated sif normal reply, code 7777, with a pulse width of 0.45 μsec as follows:

(*a*) On the radar test set SIF CODER panel, set the following controls to the indicated positions:

CODE (A, B, C, D)	7777
SUB PULSE SELECT	OFF
FUNCTION	N
LEVEL	HI
PULSE WIDTH	(.45)

(*b*) On the radar test set MARK X CODER panel, set FUNCTION to EXT HIGH, and MOD INPUT 75 Ω to OUT.

(*c*) On the radar test set CAL-CONTROL panel, set VIDEO OUT to SG MON. This makes the simulated sif reply available in demodulated form (video pulses) at the VIDEO OUT receptacle for display on the oscilloscope.

(*d*) Connect and adjust the oscilloscope to display the demodulated sif reply 500 μsec after start of sweep, using a sweep speed fast enough to measure the width of any one of the demodulated reply pulses.

(*e*) On the radar test set SIF CODER panel, readjust PULSE WIDTH so that the demodulated reply pulses are 0.45 μsec wide at half-amplitude.

(*f*) Disconnect the oscilloscope from the CAL–CONTROL panel VIDEO OUT receptacle.

(3) Tune the radar test set signal generator to the reply frequency of 1090.0 mc with an output of –40 dbm as follows:

(*a*) On the radar test set CODER SIMULATOR, set ATTENUATION to 40.0.

(*b*) On the radar test set CODER SIMULATOR, set WAVEMETER FREQUENCY to the reading corresponding to 1090.0 mc, as given in the associated wavemeter calibration chart.

(*c*) On the radar test set CAL—CONTROL panel, set METER SELECT to WM, and turn WM SENS to midposition.

(*d*) On the radar test set CODER SIMULATOR, set WAVEMETER INPUT to SIG GEN, and tune SG FREQUENCY for best "dip" (downward meter deflection) on the CAL—CONTROL panel meter. Adjust WM SENS on the CAL—CONTROL panel to keep the maximum downward deflection above zero on the meter. If the deflection cannot be kept above zero, temporarily change the CODE (A, B, C, D) settings on the SIF CODER panel from 7777 to 0000 until the best dip has been obtained. Then return the CODE (A, B, C, D) settings to 7777.

(4) On the hybrid attenuator, set ATTENUATOR to 0 (db).

(5) Set up the mode 4 word generator to provide a simulated mode 4 challenge video pulse

train beginning 182 μsec after the radar test set "0" TRIGGER (simulated radar trigger) and a simulated mode 4 gtc trigger 387 μsec after the simulated radar trigger as follows:

(*a*) On the mode 4 word generator, set the following controls to the indicated positions:

TEST WORD switches (all except No. 5)	On (up)
TEST WORD switch No. 5	Off (down)
GO — OFF — NO–GO	OFF
PRF SEL	EXT
AUXILIARY PULSE ON–OFF	OFF
AUXILIARY PULSE AM	(Fully ccw, to minimum)
AUXILIARY PULSE DELAY	(Fully cw, to maximum)
DISPARITY DL1–OFF–DL2	DL2

(*b*) On the mode 4 word generator, with TEST WORD AM. at midposition or more counterclockwise, connect W48P4 through 91–ohm series pad W48AT1 to the TEST WORD receptacle.

(*c*) Disconnect the CG–530B/U cable from the TRIGGER INPUT receptacle on the radar test set SIF CODER panel, and connect the cable to the EXT TRIG receptacle on the mode 4 word generator as shown by a broken line in figure 5–3.

(*d*) At the synchronizer, set the POWER circuit breaker to OFF and extend buffer circuit 2 card 1A2A1A7 to observe the TEST WORD (simulated mode 4 challenge video) at pin 34. Leave the synchronizer POWER circuit breaker at OFF until (*i*) below.

NOTE

Setting the synchronizer POWER circuit breaker to OFF before removing or installing a printed wiring card or a module is always a wise precaution, even when the POWER circuit breaker on the control box is at OFF.

(*e*) Connect and adjust the oscilloscope to display the simulated mode 4 challenge video at 1A2A1A7–34, using a sweep externally triggered by the positive-going "0" TRIGGER (simulated radar trigger), and fast enough to measure the delay of the first pulse of the simulated mode 4 challenge video. The amplitude of the simulated mode 4 challenge video on the oscilloscope should be 3.0 to 7.0 volts. If not, adjust TEST WORD AM. on the mode 4 word generator for an amplitude of 4.5 volts.

(*f*) On the radar test set XTAL MARK & SYNC panel, set TRIGGER DELAY RANGE to 50–750 and adjust TRIGGER DELAY COARSE and FINE so that the first pulse of the simulated mode 4 challenge video occurs 182 μsec (nominal) after the start of the oscilloscope sweep.

(*g*) Reconnect and adjust the oscilloscope to display the DISPARITY pulse (simulated mode 4 gtc trigger) at 1A2A1A7–36, using a sweep externally triggered by the simulated radar trigger as in (*e*) above, and fast enough to measure the delay of the simulated mode 4 gtc trigger.

(*h*) On the mode 4 word generator, adjust DISPARITY DL2 so that the mode 4 gtc trigger occurs 387 μsec (nominal) after the start of the oscilloscope sweep.

(*i*) At the synchronizer, disconnect the oscilloscope, reinstall buffer circuit 2 card 1A2A1A7, and set the POWER circuit breaker to ON.

(6) After the mode 4 word generator has been set up to provide simulated mode 4 challenge video and gtc triggers as in (5) above, connect and adjust the mode 4 word generator to provide a simulated mode 4 reply as follows:

(*a*) On the radar test set, disconnect the CG–530B/U cable from the MOD DRIVE receptacle on the radar test set SIF CODER panel, and connect the cable to the MODE 4 REPLY receptacle on the mode 4 word generator as shown by a broken line in figure 5–3.

(*b*) On the radar test set MARK X CODER panel, set MOD INPUT 75Ω to IN.

(*c*) On the mode 4 word generator, set MODE 4 REPLY ON–OFF to ON, and turn MODE 4 REPLY AM. approximately to midposition.

(*d*) On the radar test set CAL–CONTROL panel, set VIDEO OUT to SG MON. This makes the simulated mode 4 reply available as video pulses at the VIDEO OUT receptacle for display on the oscilloscope.

(*e*) Connect and adjust the oscilloscope to display the demodulated mode 4 reply, using a sweep externally triggered by the "0" TRIGGER (simulated radar trigger) input, and fast enough to measure the delay of the first pulse of the reply.

(*f*) On the mode 4 word generator, adjust MODE 4 REPLY DELAY so that the first pulse of the demodulated reply occurs 550 μsec (nominal) after the start of the oscilloscope sweep.

(7) After the mode 4 word generator has been set up as in (5) and (6) above, reconnect the radar test set to provide its simulated sif reply and adjust the reply delay to 500 μsec as follows:

(*a*) Disconnect the CG–530B/U cables from the EXT TRIG and MODE 4 REPLY receptacles on the mode 4 word generator, and reconnect the cables to the TRIGGER INPUT and MOD DRIVE receptacles on the radar test set SIF CODER panel as shown by unbroken lines in figure 5–3.

(*b*) On the radar test set MARK X CODER panel, set MOD INPUT 75 Ω to OUT.

(*c*) With the oscilloscope still connected to the VIDEO OUT receptacle of the radar test set CAL–CONTROL panel, the delay of the simulated sif reply can now be observed. On the radar test set XTAL MARK & SYNC panel, readjust TRIGGER DELAY COARSE and FINE so that the first pulse of the simulated sif reply occurs 500 μsec (nominal) after the start of the oscilloscope sweep.

(*d*) Disconnect the oscilloscope from the CAL–CONTROL panel VIDEO OUT receptacle.

11-5. Power and Indicator Test

(fig. 5–3)

a. Test Equipment Required. The following equipments, or suitable equivalents, are required to perform this test. For complete test equipment nomenclature and a list of test equipment operating manuals, refer to paragraph 11–3*a*.

(1) Multimeter (not shown in figure 11–1)

(2) Radar test set

(3) Test facilities set

(4) 28–volt dc power supply

b. Test Procedure. With the iff set and the required test equipment connected as shown in figure 11–1 and prepared as directed in paragraph 11–4, proceed as follows:

(1) With the POWER circuit breaker on the control box at OFF, use the multimeter as an ohmmeter to check for continuity (less than one ohm) between pins B and E (remote error indication) of EXTERNAL CHALLENGE receptacle 1J8 on the rear of the interrogator group case.

(2) On the interrogator group case power control panel, with the POWER circuit breaker at ON, depress and release the POWER lamp to check that the POWER lamp lights when depressed and goes out when released.

(3) Set the POWER circuit breaker on the control box to ON, and check that the results are as follows:

(*a*) On the interrogator group case power control panel, the POWER lamp should light and remain lighted, and the TOTAL HOURS indicator should begin operating.

(*b*) On the processor, the POWER lamp should light and remain lighted. One or more of the FAULT lamps may light momentarily, but none should remain lighted.

(*c*) On the synchronizer, the POWER lamp should light and remain lighted. One or more of the FAULT lamps may light momentarily, but none should remain lighted.

(*d*) On the receiver-trasmitter, the POWER lamp should light and remain lighted, and the TOTAL HOURS indicator should begin operating. The RCVR FAULT lamp should light for the duration of the warmup delay (approximately 1 minute) and then go out. The RF SWITCH FAULT lamp may light momentarily, but should not remain lighted. If the XMTR FAULT lamp lights, it should go out when the RCVR FAULT lamp goes out or when the FAULT RESET button is momentarily depressed.

(*e*) On the control box, the POWER lamp should light and remain lighted. The PROC

and SYN SELF TEST lamps may light momentarily with the FAULT lamps on the corresponding assemblies, but neither should remain lighted. The KIR SELF TEST lamp should not light. The R/T SELF TEST lamp should light and remain lighted until the RCVR FAULT lamp on the receiver-transmitter goes out. With the PANEL switch at OFF, none of the CODE SELECT switches should be illuminated, and the panel edge lighting lamps should be out.

(*f*) Interrogator computer power should become available at W2P1. Use the multimeter as a voltmeter to check for 28 volts dc between W2P1–31 (positive) and W2P1–34 (system ground). Then disconnect the multimeter from W2P1.

(4) On the control box, check the CODE SELECT switch and panel illumination as follows:

(*a*) Set PANEL to BRIGHT. With MODE SELECT at 1, both MODE 1 CODE SELECT switches should be illuminated, and all four panel edge lighting lamps should light to illuminate the panel lettering. The MODE 2 and MODE 3/A CODE SELECT switches should not be illuminated.

(*b*) Set MODE SELECT to 2. All four MODE 2 CODE SELECT switches should be illuminated, and the MODE 1 and MODE 3/A CODE SELECT switches should not be illuminated.

(*c*) Set MODE SELECT to 3/A. All four MODE 3/A CODE SELECT switches should be illuminated, and the MODE 1 and MODE 2 CODE select switches should not be illuminated.

(*d*) Set MODE SELECT to 4, and then unguard and turn it to LOCKOUT OVERRIDE. None of the CODE SELECT switches should light at either position.

(*e*) Return MODE SELECT to 3/A. Then switch PANEL through OFF to DIM and check that the MODE 3/A CODE SELECT switches and the panel lettering are illuminated at reduced brightness.

(*f*) Switch MODE SELECT to 2, then to 1, and check that the MODE 2 and MODE 1 CODE SELECT switches are now illuminated with essentially the same reduced brightness as the MODE 3/A CODE SELECT switches.

(*g*) Unguard and turn MODE SELECT to TEST 4. None of the CODE SELECT switches should be illuminated at this position.

(*h*) Release MODE SELECT to 1.

(5) After the R/T SELF TEST lamp on the control box goes out, use the multimeter as an ohmmeter to check for open circuit (100,000 ohms, minimum) between pins B and E (remote no-error indication) of EXTERNAL CHALLENGE receptacle 1J8 on the rear of the interrogator group case. Then disconnect the multimeter from 1J8.

(6) On the control box, depress and release LAMP TEST, and check that the CHALLENGE lamp and all four SELF TEST lamps light while LAMP TEST is depressed and go out when LAMP TEST is released. The POWER lamp may flicker once when LAMP TEST is depressed, and again when LAMP TEST is released, but should otherwise remain lighted.

(7) Connect the multimeter as a voltmeter to measure IFF set primary power between W2P1–31 (positive) and W2P1–34 (system ground), and adjust the 28–volt dc power supply for a primary power voltage of 22.5 volts.

(8) On the processor, set METER to IN and check that the meter reading settles within the center (solid green portion) of the green band.

(9) On the synchronizer, set the meter switch successively to +5, +12, and –12 and check that the meter reading settles within the center (solid green portion) of the green band. Return the meter switch to +5.

(10) Readjust the 28–volt dc power supply for a primary power voltage of 30 volts, and check that the meter readings on the processor and synchronizer are still within the center (solid green portion) of the green band.

(11) Readjust the 28–volt dc power supply for a primary power voltage of 28 volts, disconnect the multimeter from W2P1, and set the processor

METER switch and the synchronizer meter switch to OUT.

NOTE

At this point, the condition of the IFF set (turned on and warmed up) is suitable for the sif challenging test (para 11–6). If there is no reason to postpone that test, disregard (12) below, and proceed as directed in paragraph 11–6*b*, beginning with step (2).

(12) Set the POWER circuit breaker on the control box to OFF.

11-6 Mode 1, 2, and 3/A (Sif) Challenging Test (fig. 5–3)

a. Test Equipment Required. The following equipments, or suitable equivalents, are required to perform this test. For complete test equipment nomenclature and a list of test equipment operating manuals, refer to paragraph 11–3*a*.

(1) Multimeter (not shown in figure 5–3)

(2) Oscilloscope.

(3) Radar test set

(4) Test facilities set

(5) 28–volt dc power supply

b. Test Procedure. With the IFF set and the required test equipment connected as shown in figure 5–3 and prepared as directed in paragraph 11–4, proceed as follows:

NOTE

If the IFF set is already turned on and warmed up as at step (11) of the power and indicator test (para 11–5*b*), disregard (1) below, and proceed directly with (2).

(1) On the control box, set POWER to ON and wait until the R/T SELF TEST lamp goes out before proceeding.

(2) On the control box, with MODE SELECT at 1, momentarily hold CHALLENGE switch at ON and check that the CHALLENGE lamp lights while CHALLENGE is at ON and goes out when CHALLENGE is released to OFF.

(3) Temporarily simulate an external challenge enable by connecting a length of wire between pins A and C of EXTERNAL CHALLENGE receptacle 1J8 on the rear of the interrogator group case. Check that the CHALLENGE lamp on the control box lights while 1J8–A and 1J8–C are connected and goes out when those pins are disconnected by removing the length of wire.

(4) At the radar test set XTAL MARK & SYNC panel, slowly turn PRF counterclockwise (decreasing the prf) until the RADAR TRIG FAULT lamp on the synchronizer just lights and check that the SYN SELF TEST lamp on the control box is lighted.

(5) On the control box, hold CHALLENGE at ON, check that the CHALLENGE lamp does not light, and then release CHALLENGE to OFF.

(6) Using the multimeter as an ohmmeter, check for continuity (less than one ohm) between pins B and E (remote error indication) of EXTERNAL CHALLENGE receptacle 1J8.

(7) On the radar test set CAL–CONTROL panel, set METER SELECT to 500 PRF. Then, on the XTAL MARK & SYNC panel, adjust PRF for a reading of 375 (pps) on the CAL–CONTROL panel meter.

(8) Set the POWER circuit breaker on the processor to OFF and check that the PROC SELF TEST lamp on the control box is lighted.

(9) Repeat (5) and (6) above.

(10) On the control box, set PROCESSOR to BYPASS and repeat (2), above.

(11) Set the POWER circuit breaker on the processor to ON, and set the PROCESSOR switch on the control box to IN.

(12) Depress push-to-test button 1A3A3S1 on the receiver module of the receiver-transmitter and repeat (5), above. Then release 1A3A3S1.

(13) At the receiver-transmitter, connect test jack J5 of switch driver/performance monitor card 1A3A2A1 to chassis ground with a length of wire and repeat (2) and (6) above. Then disconnect the multimeter from 1J8, but leave 1A3A2A1J5 grounded until (20) below.

(14) At the front panel test adapter, first set S1 to CHAL MON DET INCIDENT PWR, and then connect the VIDEO test jack (J1) to the GND test jack (J8) with a length of wire.

(15) Repeat (5) above.

(16) At the front panel test adapter, remove the length of wire connecting the VIDEO and GND test jacks. Then disconnect the front panel test adapter from the receiver-transmitter.

(17) On the control box, hold CHALLENGE at ON.

(18) On the radar test set CAL–CONTROL panel, set VIDEO OUT to DEMOD SHAPE. This makes the mode 1 challenge pulses available at the VIDEO OUT receptacle in demodulated form (video pulses) for display on the oscilloscope.

(19) Connect and adjust the oscilloscope to display the demodulated mode 1 challenge pulses and check that two pulses are present.

NOTE

These pulses, designated P1 and P3 in order of appearance, occur approximately 428 μsec after the "0" TRIGGER (simulated radar trigger). Their pulse characteristics and spacings will be measured in (26) below, after the receiver-transmitter has been reinstalled in the interrogator group case.

(20) At the receiver-transmitter, remove the length of wire connecting 1A3A2A1J5 to chassis ground, and check that an additional pulse (designated P2) appears between P1 and P3 on the oscilloscope display.

(21) On the control box, release CHALLENGE to OFF, and set POWER to OFF.

(22) Disconnect and remove cables W39 and W40, install the receiver-transmitter in the interrogator group case, and tighten its eight front panel retaining screws.

(23) On the control box, set POWER to ON and, after the R/T SELF TEST lamp goes out, hold CHALLENGE at ON.

(24) Connect W2P1–14 (kir fault indicator enable) to W2P1–34 (system ground) to simulate the detection of an interrogator computer fault, and check that the KIR SELF TEST lamp on the control box lights and the CHALLENGE lamp remains lighted. Leave W2P1–14 and W2P1–34 connected until (34) below.

(25) Using the multimeter as a voltmeter, check that the mode 4 enable (mode 4 challenge control) level at W2P1–26 is high (+5 ±1 volts) with respect to system ground at W1P2–34. Disconnect multimeter.

(26) Adjust the oscilloscope to measure the pulse characteristics and spacings of the demodulated mode 1 challenge pulses, which should be as follows:

Pulse width at 50% amplitude . 0.8 ± 0.1 μsec
Risetime, 10% to 90% . . . . . 0.075 ± 0.025 μsec
Falltime, 90% to 10% . . . . . 0.125 ± 0.075 μsec
Leading edge spacing, P1 to P2 . 2.0 ± 0.15 μsec
Leading edge spacing, P1 to P3 . 3.0 ± 0.1 μsec

NOTE

Pulse widths are adjusted within the synchronizer: P1 and P3 by 1A2A2A5R3; and P2 by 1A2A2A5R2.

(27) On the control box, release CHALLENGE to OFF and set MODE SELECT to 2. Then hold CHALLENGE at ON and check that the CHALLENGE lamp lights.

(28) Repeat (25) above.

(29) Adjust the oscilloscope to check that three demodulated mode 2 challenge pulses are present and to measure their pulse characteristics and spacings, which should be the same as given in (26), above, except for the following:

Leading edge spacing, P1 to P3 . . . 5.0 ± 0.2 μsec

(30) On the control box, release CHALLENGE to OFF and set MODE SELECT to 3/A. Then hold CHALLENGE at ON and check that the CHALLENGE lamp lights.

(31) Repeat (25) above.

(32) Adjust the oscilloscope to check that three demodulated mode 3/A challenge pulses are present and to measure their pulse characteristics and spacings, which should be the same as given in (26), above, except for the following:

Leading edge spacing, P1 to P3 . . . 8.0 ± 0.2 μsec

(33) Repeat (25) above.

(34) Remove the length of wire connecting W2P1–14 to W2P1–34 and check that the KIR SELF TEST lamp on the control box goes out.

(35) On the radar test set CAL–CONTROL panel, set VIDEO OUT to DEMOD POWER. The pulse amplitude of the demodulated mode 3/A challenge pulses at the VIDEO OUT receptacle can now be converted to RF pulse power at the LP IN receptacle by using the LP IN demodulator calibration curve supplied with the radar test set.

(36) Adjust the oscilloscope to measure the pulse amplitudes of the P1, P2, and P3 pulses, convert the amplitudes to rf power using the LP IN demodulator calibration curve, and record the results as indicated P1 power (dbw) indicated P2 power (dbw), and indicated P3 power (dbw), respectively.

(37) Add the following attenuations and record the total as 1030-mc sum RF insertion loss of the test setup:

(*a*) The 1030–mc attenuation (in db) through the two cables (W45 and W14/W15) connecting RF SUM receptable 1J9 on the interrogator group case to RF SUM receptacle A1J2 on the hybrid attenuator;

(*b*) The 1030–mc sum channel attenuation (in db) through the hybrid attenuator, as given in the hybrid attenuator calibration data; and

(*c*) The 1030–mc attenuation (in db) through the CG–409E/U cable to the radar test set LP IN receptacle.

(38) Add the following attenuations and record the total as 1030–mc difference RF insertion loss of the test setup:

(*a*) The 1030–mc attenuation (in db) through the cable (W14/W15 and CP7/CP8) connecting RF DIFF receptacle 1J10 on the interrogator group case to ATTEN IN/RF DIFF receptacle A1J5 on the hybrid attenuator;

(*b*) The 1030–mc difference channel attenuation (in db) through the hybrid attenuator with ATTENUATOR set to 0, as given in the hybrid attenuator calibration data; and

(*c*) The 1030–mc attenuation (in db) through the CG–409E/U cable to the radar test set LP IN receptacle.

(39) Calculate the sum RF power (dbw) at RF SUM receptacle 1J9 by adding the 1030–mc sum RF insertion loss recorded in (37) above, to the indicated P1 power (dbw) recorded in (36) above. Record the sum RF power at 1J9, which should be 21.0 to 26.0 dbw.

(40) Calculate the difference RF power (dbw) at RF DIFF receptacle 1J10 by adding the 1030–mc difference RF insertion loss recorded in (38) above, to the indicated P2 power (dbw) recorded in (36) above. Record the difference RF power at 1J10, which should be equal, within ±1 db, to the sum RF power recorded in (39) above.

(41) Disconnect the oscilloscope from the VIDEO OUT receptacle of the radar test set CAL–CONTROL panel.

NOTE

At this point, the condition and connections of the IFF set and test equipment are suitable for the sif reply decoding and processing test (para 11–7). If there is no reason to postpone that test, disregard (42) below, and proceed as directed in paragraph 11–7*c*, beginning with step (2).

(42) On the control box, release CHALLENGE to OFF, set MODE SELECT to 1, and set POWER to OFF. This restores the initial settings originally made in paragraph 11–4*c*.

11-7 Mode 1,2, and 3/A (Sif) Reply Decoding and Processing Test
(fig. 5–3)

a. Test Equipment Required. The following equipments, or suitable equivalents, are required to perform this test. For complete test equipment nomenclature and a list of test equipment operating manuals, refer to paragraph 11–3*a*.

(1) Counter

(2) Multimeter (not shown in figure 5–3)

(3) Oscilloscope

(4) Radar test set

(5) Test facilities set

(6) 28–volt dc power supply

b. Preparation. If the test setup has not been changed since performing the sif challenging test (para 11–6*b*), the IFF set and test equipment are already suitably connected and prepared. If the test setup has been changed, first proceed as follows:

(1) Connect the IFF set and the required test equipment as shown in figure 5-3, except for the following:

(*a*) Do not connect cable W39, cable W40, and the front panel test adapter of the test facilities set.

(*b*) Instead, install the receiver-transmitter in the interrogator group case and tighten its eight front panel retaining screws.

(2) Turn on the test equipment and make the initial control settings and adjustments as directed in paragraph 11–4*b* through *d*.

c. Test Procedure. With the IFF set and the required test equipment suitably connected and prepared, proceed as follows:

NOTE

If the IFF set is already turned on, warmed up, and challenging in mode 3/A as at step (41) of the sif challenging test (para 11–6*b*), disregard (1), below, and proceed directly with (2).

(1) On the control box, set POWER to ON and MODE SELECT to 3/A. Then, after the R/T SELF TEST lamp goes out, hold CHALLENGE at ON.

(2) On the hybrid attenuator, set ATTENUATOR to maximum attenuation.

(3) Remove the probe from the oscilloscope CHANNEL A IN receptacle. Then connect BUFFERED VIDEO receptacle 1J3 on the interrogator group case to the CHANNEL A IN receptacle with a CG–530B/U cable, using an adapter tee (CP9/CP10/CP11) and a 75-ohm termination (AT5/AT6) at the CHANNEL A IN receptacle to terminate the cable in 75 ohms.

(4) Adjust the oscilloscope to check that a 14-pulse train of buffered receiver video pulses (representing the simulated code 7777 sif reply) is present at 1J3 and to measure the pulse characteristics of at least one of the pulses, which should be as follows:

Polarity	positive-going
Amplitude	3.0 to 5.0 volts
Pulse width	0.45 ±0.2 μsec
Risetime	0.1 μsec maximum
Falltime	0.1 μsec maximum

NOTE

The buffered receiver video pulse train is delayed from the "0" TRIGGER (simulated radar trigger) by slightly more than the 500-μsec delay established in paragraph 11–4*d*(7) (*c*).

(5) Disconnect the CG–530B/U cable from BUFFERED VIDEO receptacle 1J3 on the interrogator group case and connect the cable to DISPLAY VIDEO receptacle 1J2 to observe the IFF display video at 1J2 across 75 ohms. Adjust the oscilloscope to check that an IFF display video pulse is present and to measure its pulse characteristics, which should be as follows:

Polarity	positive-going
Amplitude	3.0 ±0.5 volts
Pulse width	1.0 ±0.1 μsec
Risetime	0.1 μsec maximum
Falltime	0.2 μsec maximum

NOTE

The IFF display video pulse occurs approximately 5 μsec after the last pulse (F2) of the buffered receiver video pulse train checked in (4) above. Its pulse width is the target present pulse width adjusted within the synchronizer by 1A2A1A5R1.

(6) On the control box, change the MODE 3/A CODE SELECT settings to 0000 and check that the IFF display video pulse disappears from the oscilloscope CHANNEL A sweep.

(7) On the control box, temporarily hold SIF REPLIES at ALL and check that the IFF display video pulse is present while SIF REPLIES is at ALL and is not present when SIF REPLIES is released to CODED. Leave SIF REPLIES at CODED.

(8) On the radar test set SIF CODER panel, change the CODE (A, B, C, D) settings to agree with the MODE 3/A CODE SELECT settings on the control box, and check that the IFF display video pulse is again present.

(9) Repeat (6) and (8) above, for successive settings of 1111, 2222, and 4444. Then return the settings to 7777.

(10) On the control box, release CHALLENGE to OFF and set MODE SELECT to 2. Then hold CHALLENGE at ON and check that the IFF display video pulse is present.

(11) On the control box, change the MODE 2 CODE SELECT settings to 0000 and check the IFF display video pulse disappears.

(12) On the radar test set SIF CODER panel, change the CODE (A, B, C, D) settings to agree with the MODE 2 CODE SELECT settings on the control box, and check that the IFF display video pulse is again present.

(13) Repeat (11) and (12) above, for successive settings of 1111, 2222, and 4444.

(14) On the radar test set SIF CODER panel, set the CODE (C, D) settings to 00 and change the CODE (A, B) settings to 73 to correspond with the MODE 1 CODE SELECT settings, 73 on the control box.

(15) On the control box, release CHALLENGE to OFF, return the MODE 2 CODE SELECT settings to 7777, and set MODE SELECT to 1. Then hold CHALLENGE at ON and check that the IFF display video pulse is present.

(16) On the control box, change the MODE 1 CODE SELECT settings to 00 and check that the IFF display video pulse disappears.

(17) On the radar test set SIF CODER panel, change the CODE (A, B) settings to agree with the MODE 1 CODE SELECT settings on the control box, and check that the IFF display video pulse is again present.

(18) Repeat (16) and (17) above, for successive settings of 11, 22, and 42. Then return the settings to 73.

(19) Set the processor POWER circuit breaker to OFF, loosen the eight front panel retaining screws which secure the processor to the interrogator group case, and pull the processor outward far enough (approximately 1 inch) to disconnect it.

(20) Check that the IFF display video pulse has disappeared from the oscilloscope CHANNEL A sweep.

(21) On the control box, set PROCESSOR to BYPASS and check that the IFF display video pulse reappears. Then set PROCESSOR to IN.

(22) Slide the processor fully into the interrogator group case, tighten its eight front panel retaining screws, and set its POWER circuit breaker to ON.

(23) On the control box, hold SIF REPLIES at ALL throughout the decoding sensitivity test of (24) through (34) below.

(24) Add the following power attenuations and record the total as 1090-mc sum RF insertion loss of the test setup (db):

(*a*) The 1090-mc attenuation (in db) through the CG–1848/U cable on the radar test set CODER SIMULATOR between the SG OUT and SG IN receptacles;

(*b*) The 1090–mc attenuation (in db) within the CODER SIMULATOR between the SG IN and LP IN receptacles;

NOTE

The radar test set calibration charts give the voltage attenuation in db between the SG IN and LP IN receptacle which must be added to the ATTENUATION dial reading.

(*c*) The 1090–mc attenuation (in db) through the CG–409E/U cable connecting the LP IN receptacle to RF IN/OUT receptacle A1J1 on the hybrid attenuator.

(*d*) The 1090–mc sum channel attenuation (in db) through the RF IN/OUT receptacle A1J2 to RF SUM receptacle A1J1 on the hybrid attenuator, as given in the hybrid attenuator calibration data; and

(*e*) The 1090–mc attenuation (in db) through the two cables (W14/W15 and W45) connecting RF SUM receptacle A1J2 on the hybrid attenuator to the RF SUM receptacle 1J9 on the interrogator group case.

(25) Determine and record the hybrid attenuator setting required for a 1090–mc signal power level 6 db lower at RF DIFF receptacle 1J10 than at RF SUM receptacle 1J9 on the interrogator group case as follows:

(*a*) Add 6 db to the 1090–mc sum channel attenuation (in db) through the hybrid attenuator, as given in the hybrid attenuator calibration data.

(*b*) To the result obtained in (*a*) above, add the 1090-mc attenuation (in db) through the two cables (W14/W15 and W45) connecting RF SUM receptacle A1J2 on the hybrid attenuator to RF SUM receptacle 1J9 on the interrogator group case.

(*c*) From the result obtained in (*b*) above, subtract the 1090–mc attenuation (in db) through the cable (W14/W15 and CP7/CP8) connecting ATTEN IN/RF DIFF receptacle A1J5 on the hybrid attenuator to RF DIFF receptacle 1J10 on the interrogator group case.

(*d*) The result obtained in (*c*) above, is the required 1090–mc difference channel attenuation (in db) through the hybrid attenuator. Obtain the corresponding ATTENUATOR setting from the hybrid attenuator calibration data and record the setting for use in (33) below.

NOTE

Leave the ATTENUATOR setting at maximum attenuation until (33) below.

(26) On the counter, set the following controls to the indicated positions:

TRIGGER VOLTS	3
FUNCTION	FREQ
SENSITIVITY	FREQ C
CLOCK FREQ	1

(27) The counter reading is the prf of the "0" TRIGGER (simulated radar trigger), which need not be changed. However, a prf which is a whole multiple of 100 (such as 400) will be more convenient in subsequent steps, where "90 percent" and "10 percent" of this prf must be calculated. Therefore, on the radar test set XTAL MARK & SYNC panel, adjust PRF (slowly) for a reading of 400.

(28) Reconnect the counter to read IFF display video prf as follows:

(*a*) Disconnect the "0" TRIGGER from the counter C (DC) receptacle by disconnecting the adapter tee (CP9/CP10/CP11) with two CG–530B/U cables attached) from the C (DC) receptacle. Leave the two CG–530B/U cables connected through the adapter tee.

(*b*) Disconnect the IFF display video from the oscilloscope by disconnecting the adapter tee from the oscilloscope CHANNEL A IN receptacle. Leave the adapter tee attached to the end of the CG–530B/U cable.

(*c*) Connect the IFF display video to the counter by connecting the adapter tee on the CG–530B/U cable to the counter C (DC) receptacle.

(*d*) Reconnect the oscilloscope probe removed in (3) above, to the oscilloscope CHANNEL A IN receptable.

(29) On the radar test set CODER SIMULATOR, slowly increase ATTENUATION until the counter reading falls to approximately 90 percent of the simulated radar trigger prf established in (27) above. Slowly vary the FREQUENCY setting to obtain the highest possible counter reading.

Then continue to increase ATTENUATION until the counter reading is equal (as nearly as possible) to 90 percent of the simulated radar trigger prf. Read the final ATTENUATION setting, which is in dbv, convert the reading to dbm by subtracting 13.0 (*for example*, 63.2 dbv -13.0 = 50.2 dbm), and record the converted reading as indicated sensitivity (dbm).

(30) Calculate the IFF set decoding sensitivity (dbm) by adding the 1090–mc sum RF insertion loss of the test setup (db) recorded in (24) above, to the indicated sensitivity (dbm) recorded in (29) above. (*For example*, 26.3 db + 50 dbm = 76.3 dbm.) Apply a minus (-) sign to the result and record it as IFF set decoding sensitivity, which should be equal to or more negative than -75 dbm.

(31) On the control box, set GTC to ON and check that the counter reading falls to 10 percent or less of the simulated radar trigger prf established in (27) above. Then set GTC to OFF.

(32) On the radar test set CODER SIMULATOR, decrease the ATTENUATION setting to 40.0.

(33) On the hybrid attenuator, turn ATTENUATOR to the setting calculated in (25) above, for a signal level 6 db lower at RF DIFF receptacle 1J10 than at RF SUM receptacle 1J9.

(34) Check that the counter reading is 10 percent or less of the simulated radar trigger prf established in (27) above.

(35) On the hybrid attenuator, return ATTENUATOR to 0 (db).

(36) Disconnect the IFF display video pulse from the counter C (DC) receptacle.

(37) On the radar test set CAL–CONTROL panel, set METER SELECT to 500 PRF. Then, on the XTAL MARK & SYNC panel, adjust PRF for a reading of 375 (pps) on the CAL–CONTROL panel meter.

(38) On the control box, release CHALLENGE to OFF and SIF REPLIES to CODED.

NOTE

At this point, the condition and connections of the IFF set and test equipment are suitable for the mode 4 challenging test (para 11–8). If there is no reason to postpone that test, disregard (39) below, and proceed as directed in paragraph 11–8*c*, beginning with step (2).

(39) On the control box, set MODE SELECT to 1, and POWER to OFF. This restores the initial settings originally made in paragraph 11–4*c*.

11-8 Mode 4 Challenging Test

(fig. 5–3)

a. Test Equipment Required. The following equipments, or suitable equivalents, are required to perform this test. For complete test equipment nomenclature and a list of test equipment operating manuals, refer to paragraph 11–3*a*.

(1) Counter

(2) Mode 4 word generator

(3) Multimeter (not shown in figure 5–3)

(4) Oscilloscope

(5) Radar test set

(6) Test facilities set

(7) 28-volt dc power supply

b. Preparation. If the test setup has not been changed since performing the sif reply decoding and processing test (para 11–7*c*), the IFF set and test equipment are already suitably connected and prepared. If the test setup has been changed, first proceed as follows:

(1) Connect the IFF set and the required test equipment as shown in figure 5–3, except for the following:

(*a*) Do not connect cable W39, cable W40, and the front panel test adapter of the test facilities set.

(*b*) Instead, install the receiver-transmitter in the interrogator group case and tighten its eight front panel retaining screws.

(*c*) Do not connect the "0" TRIGGER to the counter FREQ A receptacle. The adapter tee (CP9/CP10/CP11) shown joining the two CG-530B/U ("0" TRIGGER) cables at the counter will be connected to the B (DC) receptacle during the test procedure.

(2) Turn on the test equipment as directed in paragraph 11-4*b*.

(3) Make the initial IFF set control settings specified in paragraph 11-4*c*.

(4) Set the "0" TRIGGER (simulated radar trigger) prf to 375 pps as directed in paragraph 11-4*d*(1).

(5) On the hybrid attenuator, set ATTENUATOR to 0 (db).

c. Test Procedure. With the IFF set and the required test equipment suitably connected and prepared, proceed as follows:

NOTE

If the IFF set is already turned on and warmed up as at step (38) of the sif reply decoding and processing test (para 11-7*c*), disregard (1) below, and proceed directly with (2).

(1) On the control box, set POWER to ON.

(2) Set up the mode 4 word generator to provide simulated mode 4 challenge video and gtc triggers as directed in paragraph 11-4*d*(5) (*c*) through (*f*) and (*i*).

(4) With W48P3 (mode 4 pretrigger) connected to a 75-ohm termination (AT5/AT6) through an adapter tee (CP9/CP10/CP11), connect the oscilloscope to W48P3 through the adapter tee to observe the mode 4 pretrigger across 75 ohms. Adjust the oscilloscope to check that a mode 4 pretrigger is present and to measure its pulse characteristics, which should be as follows:

Polarity	positive-going
Amplitude	1.5 to 5.0 volts
Pulse width	0.5 to 10.0 μsec
Risetime	0.1 μsec maximum
Falltime	0.2 μsec maximum

(4) Connect the counter to measure the delay of the mode 4 pretrigger from the "0" TRIGGER (simulated radar trigger) as follows:

(*a*) Connect the "0" TRIGGER adapter tee (CP9/CP10/CP11, shown at the C (DC) receptacle in figure 5-3) to the B (DC) receptacle, leaving both CG-530B/U cables connected through the adapter tee.

(*b*) Disconnect the oscilloscope from the adapter tee on W48P3 and connect W48P3 to the counter B (DC) receptacle, using the adapter tee and 75-ohm termination at the B (DC) receptacle to terminate the mode 4 pretrigger in 75 ohms.

(5) On the counter, set the following controls to the indicated positions:

FUNCTION	TIME B C
Time base (outer)	CLOCK FREQ (CPS) -10^7
DISPLAY	00 (fully counterclockwise)
Mode selector	SEP
B TRIGGER VOLTS (inner)	+4
B MULTIPLIER	3
B SLOPE	+
C TRIGGER VOLTS (inner)	+2
C MULTIPLIER	1
C SLOPE	+

(6) On the counter, depress and release RESET to obtain a reading of mode 4 pretrigger delay, which should be 14.5 ± 0.2 μsec.

(7) On the control box, set MODE SELECT to 4, and hold CHALLENGE at ON to challenge in mode 4. Check that the CHALLENGE lamp lights.

(8) On the radar set CAL—CONTROL panel, set VIDEO OUT TO DEMOD SHAPE. This makes the mode 4 challenge pulse train available at the VIDEO OUT receptacle in demodulated form (video pulses) for display on the oscilloscope.

(9) Connect and adjust the oscilloscope to display the demodulated mode 4 challenge pulse train (37 pulses spaced at nominal intervals of 2 μsec) and to measure the pulse characteristics within the train and the spacing between the leading edges of the fourth and fifth pulses, which should be as follows:

Pulse width at 50% amplitude ____0.5 ±0 μsec
Risetime, 10% to 90% _____0.075 ±0.025 μsec
Falltime, 90% to 10% _____0.125 ±0.075 μsec
Leading edge spacing between
fourth and fifth pulses _____2.0 ±0.15 μsec

NOTE

Pulse width is adjusted within the synchronizer by 1A2A2A5R1. This pulse train represents the mode 4 word generator TEST WORD (with an isls pulse inserted), and the pulse train delay from the "0" TRIGGER (simulated radar trigger) is therefore slightly more than the 182-μsec delay established in paragraph 11-4*d*(5)(*f*).

(10) Disconnect the oscilloscope from the radar test set CAL-CONTROL panel VIDEO OUT receptacle.

(11) Momentarily simulate the detection of an interrogator computer fault by connecting W2P1-14 (kir fault indicator enable) to W2P1-34 (system ground) with a length of wire. Check that the KIR SELF TEST lamp on the control box lights and that the CHALLENGE lamp goes out. Then disconnect W2P1-14 from W2P1-34 by removing the length of wire.

(12) Using the multimeter as a voltmeter check that the mode 4 enable (mode 4 challenge control) level at W2P1-26 is low (0.0 ± 0.5 volt) with respect to W2P1-34 (system ground).

(13) Disconnect the multimeter from W2P1-26, but leave one multimeter test lead connected to W2P1-34 (system ground).

NOTE

In (14) through (19) below, the multimeter is to be used as an ohm-meter with one test lead grounded at W2P1-34 to check for grounds and open circuits at specified pins of W2P1. To check for a ground or open circuit, connect the free lead of the multimeter to the specified pin and note the indication. A ground is present if the indication is less than one ohm. An open circuit is present if the indication is 100,000 ohms or greater.

(14) Check for an open circuit at W2P1-23 (mode 4 noise alarm override).

(15) On the control box, unguard MODE SELECT and hold it at LOCKOUT OVERRIDE. Check that the CHALLENGE lamp is lighted, and check for a ground at W2P1-23. Then release MODE SELECT to 4.

(16) Check for an open circuit at W2P1-19 (mode 4 test enable).

(17) On the control box, unguard MODE SELECT and hold it at TEST 4. Check that the CHALLENGE lamp is lighted, check for a ground at W2P1-19, and check for an open circuit at W2P1-24 (verification bit 2). Then release CHALLENGE to OFF and MODE SELECT to 1.

(18) On the control box, set MODE 4 to each of its four positions in turn (unguarding to reach CODE HOLD and ZERO), and check for the following combinations of grounds and open circuits at each of the indicated pins:

	MODE 4 switch setting			
Pin	*CODE HOLD*	*A*	*B*	*ZERO*
W2P1-9	Open circuit	Open circuit	Ground	Open circuit
W2P1-32	Ground	Open circuit	Open circuit	Open circuit
W2P1-33	Ground	Ground	Ground	Open circuit
W2P1-37	Ground	Open circuit	Open circuit	Open circuit

(19) Check for a ground at W2P1-20 (chassis ground). This verifies system ground to chassis ground continuity.

(20) Disconnect the multimeter from W2P1-20 and W2P1-34 and reconnect it to check for interlock continuity (less than one ohm) between W2P1-12 and W2P1-13.

(21) Disconnect the multimeter from W2P1.

(22) Disconnect the mode 4 pretrigger from the counter by disconnecting the assembly of

W48P3, adapter tee, and 75-ohm termination from the C (DC) receptacle.

(23) Disconnect the "0" TRIGGER from the counter by disconnecting the assembly of adapter tee and two CG–530B/U cables from the B (DC) receptacle. Leave the two CG–530B/U cables connected through the adapter tee.

NOTE

At this point, the condition and connections of the IFF set and test equipment are suitable for the mode 4 reply decoding and processing test (para 11–9). If there is no reason to postpone that test, disregard (24) below, and proceed as directed in paragraph 11–9*c*, beginning with step (2).

(24) On the control box, set POWER to OFF. This restores the initial settings originally made in paragraph 11–4*c*.

11-9 Mode 4 Reply Decoding and Processing Test (fig. 5–3)

a. Test Equipment Required. The following equipments, or suitable equivalents, are required to perform this test. For complete test equipment nomenclature and a list of test equipment operating manuals, refer to paragraph 11–3*a*.

(1) Mode 4 word generator.

(2) Oscilloscope

(3) Radar test set

(4) Test facilities set

(5) 28-volt dc power supply

b. Preparation. If the test setup has not been changed since performing the mode 4 challenging test (para 11–8*c*), the IFF set and test equipment are already suitably connected and prepared. If the test setup has been changed, first proceed as follows:

(1) Connect the IFF set and the required test equipment as shown in figure 5–3, except for the following:

(*a*) Do not connect cable W39, cable W40, and the front panel adapter of the test facilities set.

(*b*) Instead, install the receiver-transmitter in the interrogator group case and tighten its eight front panel retaining screws.

(2) Turn on the test equipment as directed in paragraph 11–4*b*.

(3) Make the initial IFF set control settings specified in paragraph 11–4*c*.

(4) Set the "0" TRIGGER (simulated radar trigger) prf to 375 pps as directed in paragraphs 11–4*d*(1).

(5) Set up the mode 4 word generator to provide simulated mode 4 challenge video and gtc triggers as directed in paragraph 11–4*d*(5) (*c*) through (*f*) and (*i*).

c. Test Procedure. With the IFF set and the required test equipment suitably connected and prepared, proceed as follows:

NOTE

If the IFF set is already turned on and warmed up as at step (23) of the mode 4 challenging test (para 11–8*c*), disregard (1) below, and proceed directly with (2).

(1) On the control box, set POWER to ON. Then proceed with (2) through (4) below, while waiting for the R/T SELF TEST lamp to go out.

(2) Connect the mode 4 word generator to provide a simulated mode 4 reply as directed in paragraph 11–4*d*(6) (*a*) and (*b*).

(3) On the hybrid attenuator, set ATTENUATOR to maximum attenuation.

(4) Remove the probe from the oscilloscope CHANNEL A IN receptacle. Then connect BUFFERED VIDEO receptacle 1J3 on the interrogator group case to the oscilloscope CHANNEL A IN receptacle with a CG–530B/U cable, using an adapter tee (CP9/CP10/CP11) and a 75–ohm termination (AT5/AT6) at the CHANNEL A IN receptacle to terminate the cable in 75 ohms.

(5) On the control box, set MODE SELECT to 4 and hold CHALLENGE at ON.

(6) Adjust the oscilloscope to check that three buffered receiver video pulses (representing the simulated mode 4 reply) are present at 1J3.

NOTE

The three buffered receiver video pulses are delayed from the "0" TRIGGER (simulated radar trigger) by slightly more than the 570-μsec delay established in paragraph 11–4*d*(6) (*f*).

(7) Connect W48P2 (triple pulse decoded video) to W48P6 (mode 4 time decoded video), using an appropriate adapter (W39CP1 or W39CP2). This returns the triple pulse decoded video to the synchronizer as mode 4 time decoded video and thereby terminates the triple pulse decoded video in 91 ohms ± 10 percent.

(8) At the synchronizer, set POWER to OFF and extend buffer circuit 1 card 1A2A1A8 for access to mode 4 time decoded video on pin 32. Then set POWER to ON.

(9) Connect the oscilloscope CHANNEL B probe to 1A2A1A8–32, and adjust the oscilloscope to check that a mode 4 time decoded video pulse is present and to measure its pulse characteristics, which should be as follows:

Polarity	positive-going
Amplitude	3.0 to 5.0 volts
Pulse width	0.5 ± 0.2 μsec
Risetime	0.1 μsec maximum
Falltime	0.1 μsec maximum

NOTE

This mode 4 time decoded video pulse is actually the triple pulse decoded video pulse at W48P2 and occurs approximately in coincidence with the third buffered receiver video pulse on the oscilloscope CHANNEL A sweep.

(10) Disconnect the CG–530B/U cable from BUFFERED VIDEO receptacle 1J3 and connect the cable to DISPLAY VIDEO receptacle 1J2 to observe the IFF display video pulse across 75 ohms on the oscilloscope CHANNEL A sweep.

(11) Adjust the oscilloscope to check that an IFF display video pulse is present at 1J2 and to measure its pulse characteristics, which should be as follows:

Polarity	positive-going
Amplitude	5.0 ± 0.5 volts
Pulse width	5.0 ± 0.5 μsec
Risetime	0.4 μsec maximum
Falltime	1.0 μsec maximum

NOTE

The IFF display video pulse occurs approximately 5 μsec later than the mode 4 time decoded video pulse on the oscilloscope CHANNEL B sweep. Its amplitude and pulse width are the friend pulse amplitude and width adjusted within the synchronizer by 1A2A1A5R2 and 1A2A1A5R3, respectively.

(12) On the control box, set PROCESSOR to BYPASS and check that the IFF display video pulse amplitude and width decrease to the target present pulse amplitude (3.0 ± 0.5 volts) and width (1.0 ± 0.1 μsec) previously checked in paragraph 11–7*c* (5).

(13) On the control box, set PROCESSOR to IN and release CHALLENGE to OFF.

(14) At the synchronizer, disconnect the oscilloscope CHANNEL B probe, set POWER to OFF, and reinstall buffer circuit 1 card 1A2A1A8. Then set POWER to ON.

NOTE

At this point, the condition and connections of the IFF set and test equipment are suitable for the test target mode test (para 11–10). If there is no reason to postpone that test, disregard (15) below, and proceed as directed in paragraph 11–10*c*, beginning with step (2).

(15) On the control box, set POWER to OFF and MODE SELECT to 1. This restores the initial settings originally made in paragraph 11–4 *c*.

11-10 Test Target Mode Test

(fig. 5–3)

a. Test Equipment Required. The following equipments, or suitable equivalents, are required to

perform this test. For complete test equipment nomenclature and a list of test equipment operating manuals, refer to paragraph 11–3*a*.

(1) Oscilloscope
(2) Radar test set
(3) Test facilities set
(4) 28-volt dc power supply

b. Preparation. If the test setup has not been changed since performing the mode 4 reply decoding and processing test (para 11–9*c*), the IFF set and test equipment are already suitably connected and prepared. If the test setup has been changed, first proceed as follows:

(1) Connect the IFF set and the required test equipment as shown in figure 5–3, except for the following:

(*a*) Do not connect cable W39, cable W40, and the front panel adapter of the test facilities set.

(*b*) Instead, install the receiver-transmitter in the interrogator group case and tighten its eight front panel retaining screws.

(2) Turn on the test equipment as directed in paragraph 11–4*b*.

(3) Make the initial IFF set control settings specified in paragraph 11–4*c*.

(4) Set the "0" TRIGGER (simulated radar trigger) prf to 375 pps as directed in paragraph 11–4*d*(1).

(5) Remove the probe from the oscilloscope CHANNEL A IN receptacle. Then connect DISPLAY VIDEO receptacle 1J2 on the interrogator group case to the oscilloscope CHANNEL A IN receptacle with a CG–530B/U cable, using an adapter tee (CP9/CP10/CP11) and a 75-ohm termination (AT5/AT6) at the CHANNEL A IN receptacle to terminate the cable in 75 ohms.

c. Test Procedure. With the IFF set and the required test equipment suitably connected and prepared, proceed as follows:

NOTE

If the IFF set is already turned on and warmed up as at step (14) of the mode 4 reply decoding and processing test (para 11–9*c*), disregard (1) below, and proceed directly with (2).

(1) On the control box, set POWER to ON. Then continue with the remaining steps below. It is not necessary to wait until the R/T SELF TEST lamp goes out.

(2) Connect the oscilloscope CHANNEL B probe to the synchronizer at 1A2A4A3J1–6 (processor start pretrigger). Adjust the oscilloscope to display the processor start pretrigger near the start of a 20-μsec/cm sweep delayed approximately 450 μsec from the "0" TRIGGER (simulated radar trigger), so that the IFF display video on the CHANNEL A sweep can be examined throughout an interval of at least 188 μsec immediately following the processor start pretrigger.

(3) On the control box, hold CHALLENGE at TEST and check that a train of IFF display video pulses appears, sliding smoothly rightward across the CHANNEL A sweep. Each pulse should appear within 6 to 8 μsec after the processor start pretrigger and then disappear approximately 188 μsec later, so that there are never less than two nor more than three IFF display video pulses visible on the CHANNEL A sweep at any one time.

(4) Adjust the oscilloscope to examine one of the sliding IFF display pulses in detail, and check that it is a superimposed combination of two different pulse shapes: the friend pulse shape (5.0 ± 0.5 volts; 5.0 ± 0.5 μsec) previously checked in paragraph 11–9*c* (11); and the target present pulse shape (3.0 ± 0.5 volts; 1.0 ± 0.1 μsec) previously checked in paragraph 11–7*c* (5).

(5) On the control box, release CHALLENGE to OFF and set POWER to OFF.

(6) Disconnect the oscilloscope CHANNEL B probe from the synchronizer. Then disconnect the CG–530B/U cable, adapter tee, and 75–ohm termination from the CHANNEL A IN receptacle, and reconnect the CHANNEL A probe.

(7) Turn off all test equipment and disconnect it from the IFF set.

(8) Install the synchronizer in the interrogator group case and tighten its eight front panel retaining screws.

(9) Tag the IFF set for return to stock and reissue in accordance with the applicable procedures of the depot performing the test (para 11–2*a*).

CHAPTER 12

FOLDOUT DRAWINGS

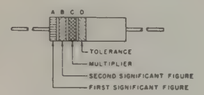
12-1. General

This chapter contains the foldout-size illustrations which have been referenced in other chapters. The first illustration, figure 12–1, shows and explains the color code markings for MIL-STD resistors and capacitors. The remaining illustrations are presented in the order referenced, as follows:

Figure No.	*Content*
12–2	IFF set, system functional block diagram
12–3	IFF set interconnection wiring diagram
12–4	Control circuits, functional block diagram
12–5	Interrogator group case schematic diagram
12–6	Control box interconnection block diagram
12–7	Lamp driver card, schematic diagram

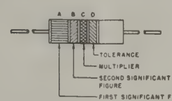
COLOR CODE MARKING FOR MILITARY STANDARD RESISTORS

COMPOSITION-TYPE RESISTORS



BAND A—Equal Width Band Signifies Composition-Type

WIREWOUND-TYPE RESISTORS

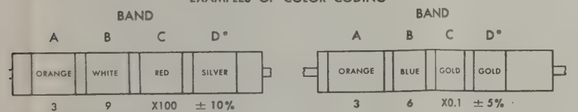


BAND A—Double Width Signifies Wire-wound Resistor

COLOR CODE TABLE

BAND A		BAND B		BAND C		BAND D*	
COLOR	FIRST SIGNIFICANT FIGURE	COLOR	SECOND SIGNIFICANT FIGURE	COLOR	MULTIPLIER	COLOR	RESISTANCE TOLERANCE (PERCENT)
BLACK	0	BLACK	0	BLACK	1		
BROWN	1	BROWN	1	BROWN	10		
RED	2	RED	2	RED	100		
ORANGE	3	ORANGE	3	ORANGE	1,000		
YELLOW	4	YELLOW	4	YELLOW	10,000	SILVER	± 10
GREEN	5	GREEN	5	GREEN	100,000	GOLD	± 5
BLUE	6	BLUE	6	BLUE	1,000,000		
PURPLE (VIOLET)	7	PURPLE (VIOLET)	7				
GRAY	8	GRAY	8	SILVER	0.01		
WHITE	9	WHITE	9	GOLD	0.1		

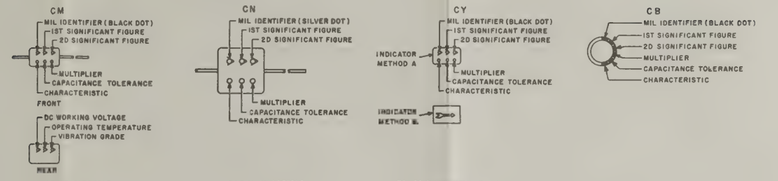
EXAMPLES OF COLOR CODING



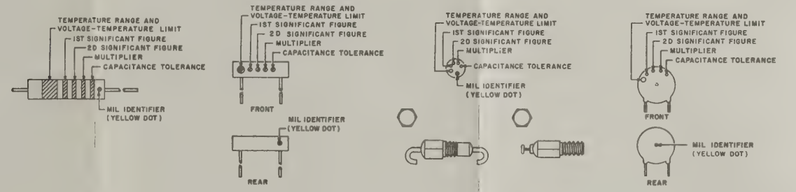
*If Band D is omitted, the resistor tolerance is ±20%, and the resistor is not Mil-Std.

COLOR CODE MARKING FOR MILITARY STANDARD CAPACITORS

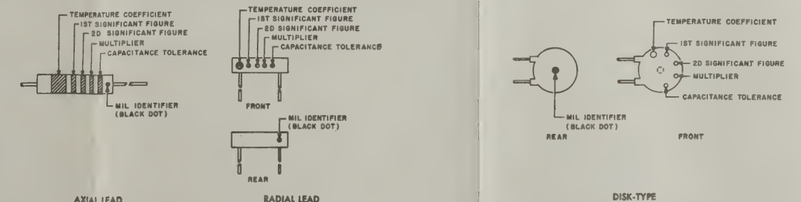
GROUP I Capacitors, Fixed, Various-Dielectrics, Styles CM, CN, CY, and CB



GROUP II Capacitors, Fixed Ceramic-Dielectric (General Purpose) Style CK



GROUP III Capacitors, Fixed, Ceramic-Dielectric (Temperature Compensating) Style CC



COLOR CODE TABLES

TABLE I — For use with Group I, Styles CM, CN, CY and CB

COLOR	MIL ID	1st SIG FIG	2nd SIG FIG	MULTIPLIER[1]	CAPACITANCE TOLERANCE				CHARACTERISTIC[2]				DC WORKING VOLTAGE	OPERATING TEMP. RANGE	VIBRATION GRADE
					CM	CN	CY	CB	CM	CN	CY	CB	CM	CM	CM
BLACK	CM, CY CB	0	0	1			± 20%	± 20%		A				−55° to +70°C	10–55 cps
BROWN		1	1	10					B	L	B				
RED		2	2	100	± 2%		± 2%	± 2%	C		C			−55° to +85°C	
ORANGE		3	3	1,000		± 30%			D		D		300		
YELLOW		4	4	10,000					E					−55° to +125°C	10–2,000 cps
GREEN		5	5		± 5%				F				500		
BLUE		6	6											−55° to +150°C	
PURPLE (VIOLET)		7	7												
GREY		8	8												
WHITE		9	9												
GOLD				0.1			± 5%	± 5%							
SILVER	CN				± 10%	± 10%	± 10%	± 10%							

TABLE II — For use with Group II, General Purpose, Style CK

COLOR	TEMP. RANGE AND VOLTAGE — TEMP. LIMITS[3]	1st SIG FIG	2nd SIG FIG	MULTIPLIER[1]	CAPACITANCE TOLERANCE	MIL ID
BLACK		0	0	1	± 20%	
BROWN	AW	1	1	10	± 10%	
RED	AX	2	2	100		
ORANGE	BX	3	3	1,000		
YELLOW	AY	4	4	10,000		CK
GREEN	CZ	5	5			
BLUE	BY	6	6			
PURPLE (VIOLET)		7	7			
GREY		8	8			
WHITE		9	9			
GOLD						
SILVER						

TABLE III — For use with Group III, Temperature Compensating, Style CC

COLOR	TEMPERATURE COEFFICIENT[4]	1st SIG FIG	2nd SIG FIG	MULTIPLIER[1]	CAPACITANCE TOLERANCE		MIL ID
					Capacitances over 10uuf	Capacitances 10uuf or less	
BLACK	0	0	0	1		± 2.0uuf	CC
BROWN	−30	1	1	10	± 1%		
RED	−80	2	2	100	± 2%	± 0.25uuf	
ORANGE	−150	3	3	1,000			
YELLOW	−220	4	4				
GREEN	−330	5	5		± 5%	± 0.5uuf	
BLUE	−470	6	6				
PURPLE (VIOLET)	−750	7	7				
GREY		8	8	0.01			
WHITE		9	9	0.1	± 10%		
GOLD	+100					± 1.0uuf	
SILVER							

1. The multiplier is the number by which the two significant (SIG) figures are multiplied to obtain the capacitance in uuf.
2. Letters indicate the Characteristics designated in applicable specifications: MIL–C–5, MIL–C–91, MIL–C–11272, and MIL–C–10950 respectively.
3. Letters indicate the temperature range and voltage-temperature limits designated in MIL–C–11015.
4. Temperature coefficient in parts per million per degree centigrade.

STD–CE

Figure 12–1. Color code markings for MIL–STD resistors and capacitors.

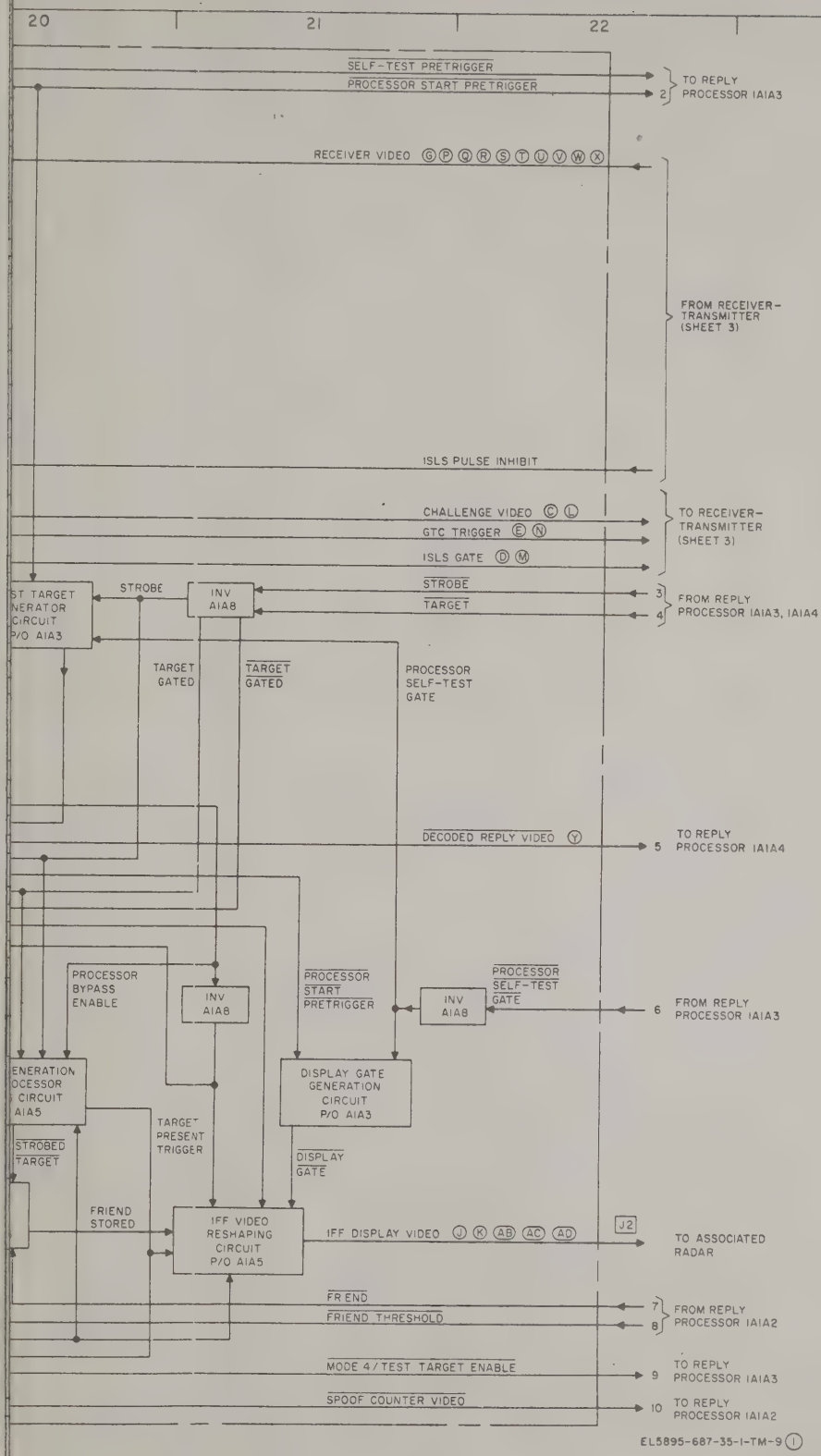


Figure 12–2 (1). IFF set, system functional block diagram (sheet 1 of 3).

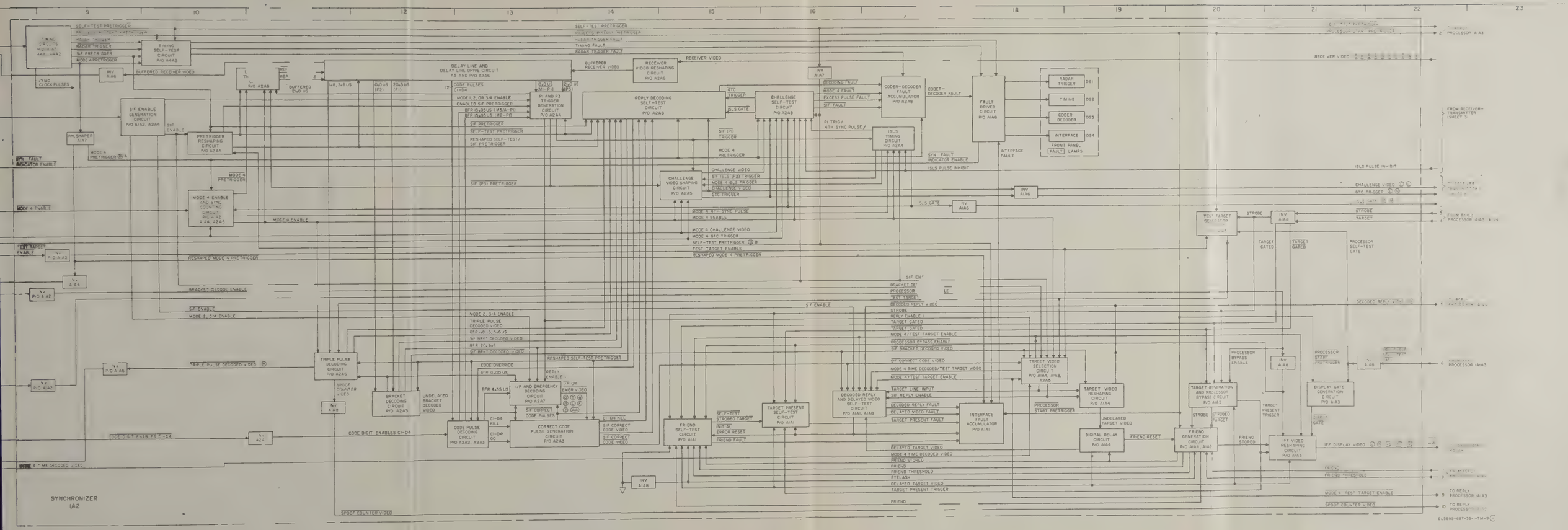
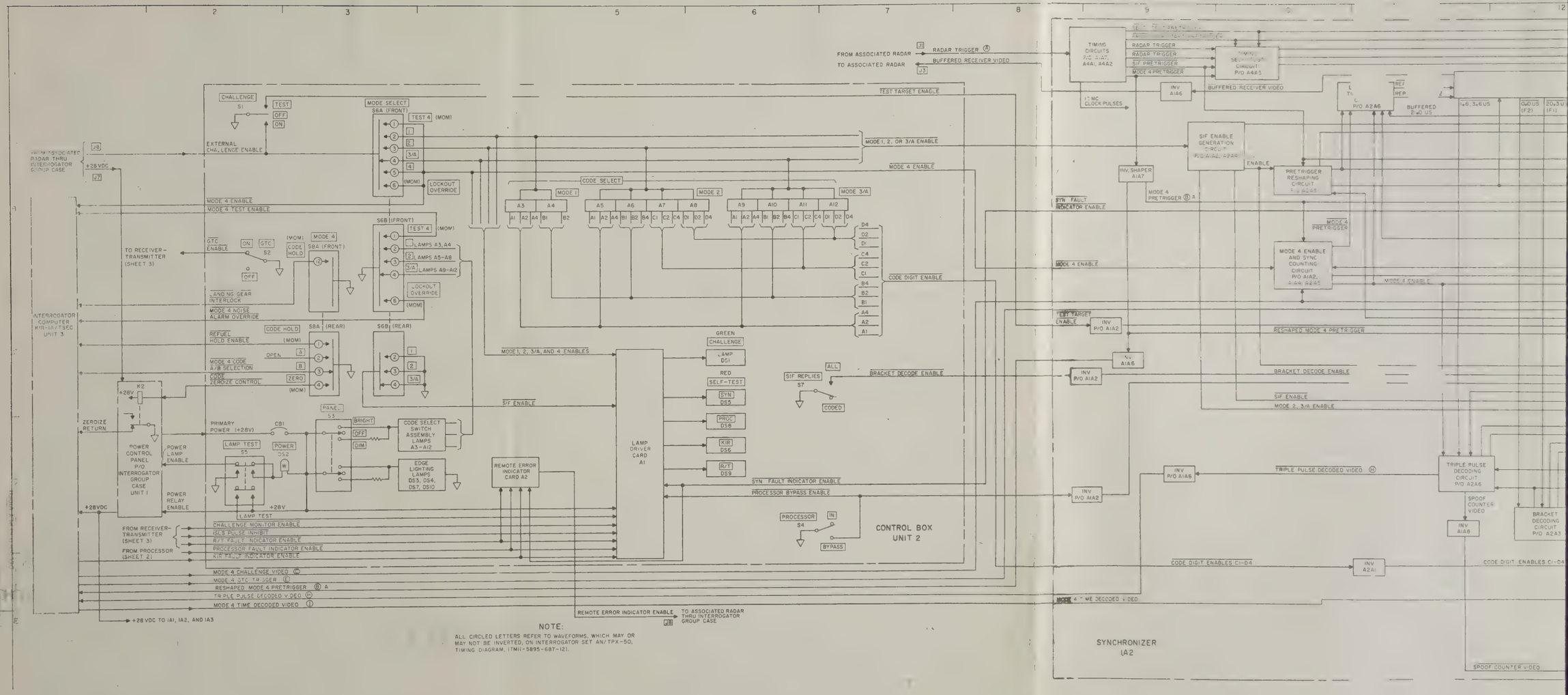
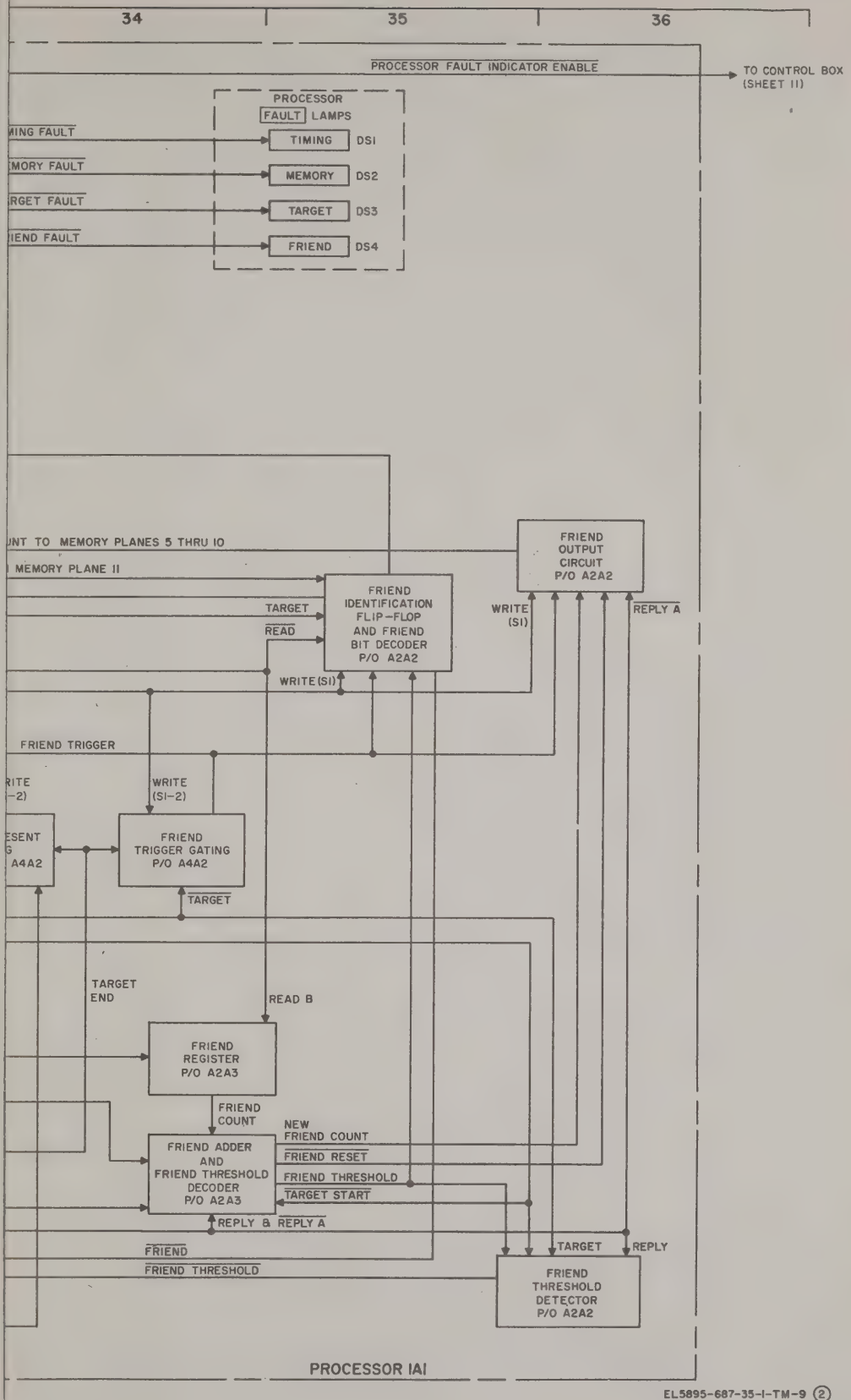

SYNCHRONIZER
1A2
TIMING CIRCUITS P/O A1A7, A4B, A4B2
TIMING SELF-TEST CIRCUIT P/O A4A3
17 MC CLOCK PULSES
RAIN SHAPER A1A7
SIF ENABLE GENERATION CIRCUIT P/O A1A2, A2A4
PRETRIGGER RESHAPING CIRCUIT P/O A2A5
MODE 4 ENABLE AND SYNC COUNTING CIRCUIT P/O A2A2, A2A4, A2A5
DELAY LINE AND DELAY LINE DRIVE CIRCUIT A5 AND P/O A2A6
RECEIVER VIDEO RESHAPING CIRCUIT P/O A2A6
REPLY DECODING SELF-TEST CIRCUIT P/O A2A8
P1 AND P3 TRIGGER GENERATION CIRCUIT P/O A2A4
CHALLENGE SELF-TEST CIRCUIT P/O A2A8
CODER-DECODER FAULT ACCUMULATOR P/O A2A8
ISLS TIMING CIRCUIT P/O A2A4
FAULT DRIVER CIRCUIT P/O A1A8
CHALLENGE VIDEO SHAPING CIRCUIT P/O A2A5
TRIPLE PULSE DECODING CIRCUIT P/O A2A6
BRACKET DECODING CIRCUIT P/O A2A3
CODE PULSE DECODING CIRCUIT P/O A2A2, A2A3
CORRECT CODE PULSE GENERATION CIRCUIT P/O A2A3
I/P AND EMERGENCY DECODING CIRCUIT P/O A2A7
FRIEND SELF-TEST CIRCUIT P/O A1A1
TARGET PRESENT SELF-TEST CIRCUIT P/O A1A1
DECODED REPLY AND DELAYED VIDEO SELF-TEST CIRCUIT P/O A1A1, A1A8
INTERFACE FAULT ACCUMULATOR P/O A1A1
TARGET VIDEO SELECTION CIRCUIT P/O A1A4, A1A5, A2A5
TARGET VIDEO RESHAPING CIRCUIT P/O A1A4
DIGITAL DELAY CIRCUIT P/O A1A4
TARGET GENERATION AND PROCESSOR BYPASS CIRCUIT P/O A1A5
FRIEND GENERATION CIRCUIT P/O A1A4, A1A5
DISPLAY GATE GENERATION CIRCUIT P/O A1A3
IFF VIDEO RESHAPING CIRCUIT P/O A1A5
RADAR TRIGGER
TIMING
CODER DECODER
INTERFACE
FRONT PANEL FAULT LAMPS
DS1
DS2
DS3
DS4
TO/FROM PROCESSOR A1A3
FROM RECEIVER-TRANSMITTER (SHEET 3)
TO REPLY PROCESSOR 1A1A3
E-5895-687-35-1-TM-9

Figure 12–2 (1). IFF set, system functional block diagram (sheet 1 of 3).


CONTROL BOX UNIT 2
SYNCHRONIZER IA2
NOTE:
ALL CIRCLED LETTERS REFER TO WAVEFORMS, WHICH MAY OR MAY NOT BE INVERTED, ON INTERROGATOR SET AN/TPX-50, TIMING DIAGRAM, ITMII-5895-687-12).
CHALLENGE S1
MODE SELECT S6A (FRONT)
S6B (FRONT)
S6A (REAR)
S6B (REAR)
CODE SELECT
MODE 1
MODE 2
MODE 3/A
MODE 4
S2
S3
S4
S7
K2
CB1
LAMP TEST S5
POWER DS2
LAMP DRIVER CARD A1
REMOTE ERROR INDICATOR CARD A2
POWER CONTROL PANEL P/O INTERROGATOR GROUP CASE UNIT 1
CODE SELECT SWITCH ASSEMBLY LAMPS A3-A12
EDGE LIGHTING LAMPS DS3, DS4, DS7, DS10
GREEN CHALLENGE LAMP DS1
RED SELF-TEST
SYN DS5
PROC DS8
KIR DS6
R/T DS9
TIMING CIRCUITS P/O A1A7, A4A1, A4A2
SIF ENABLE GENERATION CIRCUIT P/O A1A2, A2A6
PRETRIGGER RESHAPING CIRCUIT P/O A2A6
MODE 4 ENABLE AND SYNC COUNTING CIRCUIT P/O A1A2, A1A4, A2A5
TRIPLE PULSE DECODING CIRCUIT P/O A2A6
BRACKET DECODING CIRCUIT P/O A2A3
INV A1A6
INV P/O A1A2
INV A2A1
INV SHAPER A1A7
FROM ASSOCIATED RADAR
TO ASSOCIATED RADAR
RADAR TRIGGER
BUFFERED RECEIVER VIDEO
TEST TARGET ENABLE
MODE 1, 2, OR 3/A ENABLE
MODE 4 ENABLE
CODE DIGIT ENABLE
BRACKET DECODE ENABLE
SIF ENABLE
MODE 1, 2, 3/A, AND 4 ENABLES
SYN FAULT INDICATOR ENABLE
PROCESSOR BYPASS ENABLE
RESHAPED MODE 4 PRETRIGGER
TRIPLE PULSE DECODED VIDEO
SPOOF COUNTER VIDEO
CODE DIGIT ENABLES C1-D4
MODE 4 TIME DECODED VIDEO
REMOTE ERROR INDICATOR ENABLE
TO ASSOCIATED RADAR THRU INTERROGATOR GROUP CASE
+28VDC TO IA1, IA2, AND IA3



EL5895-687-35-1-TM-9 (2)

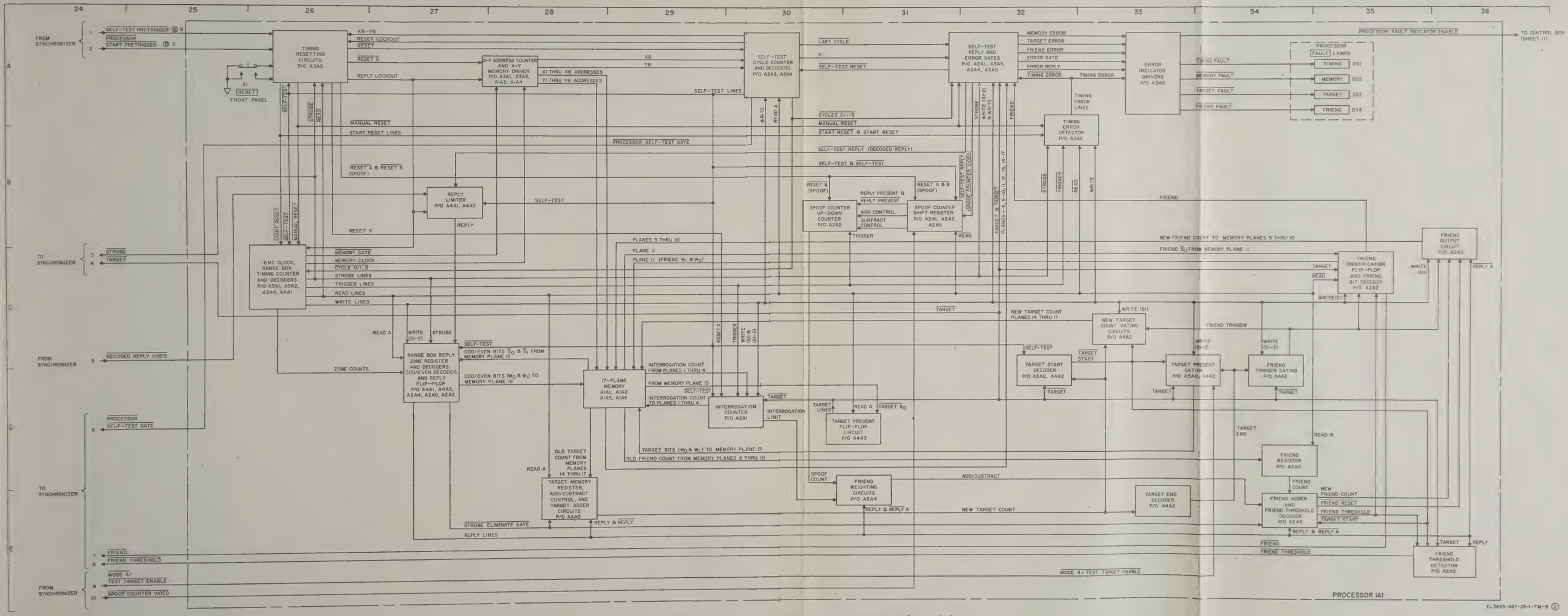
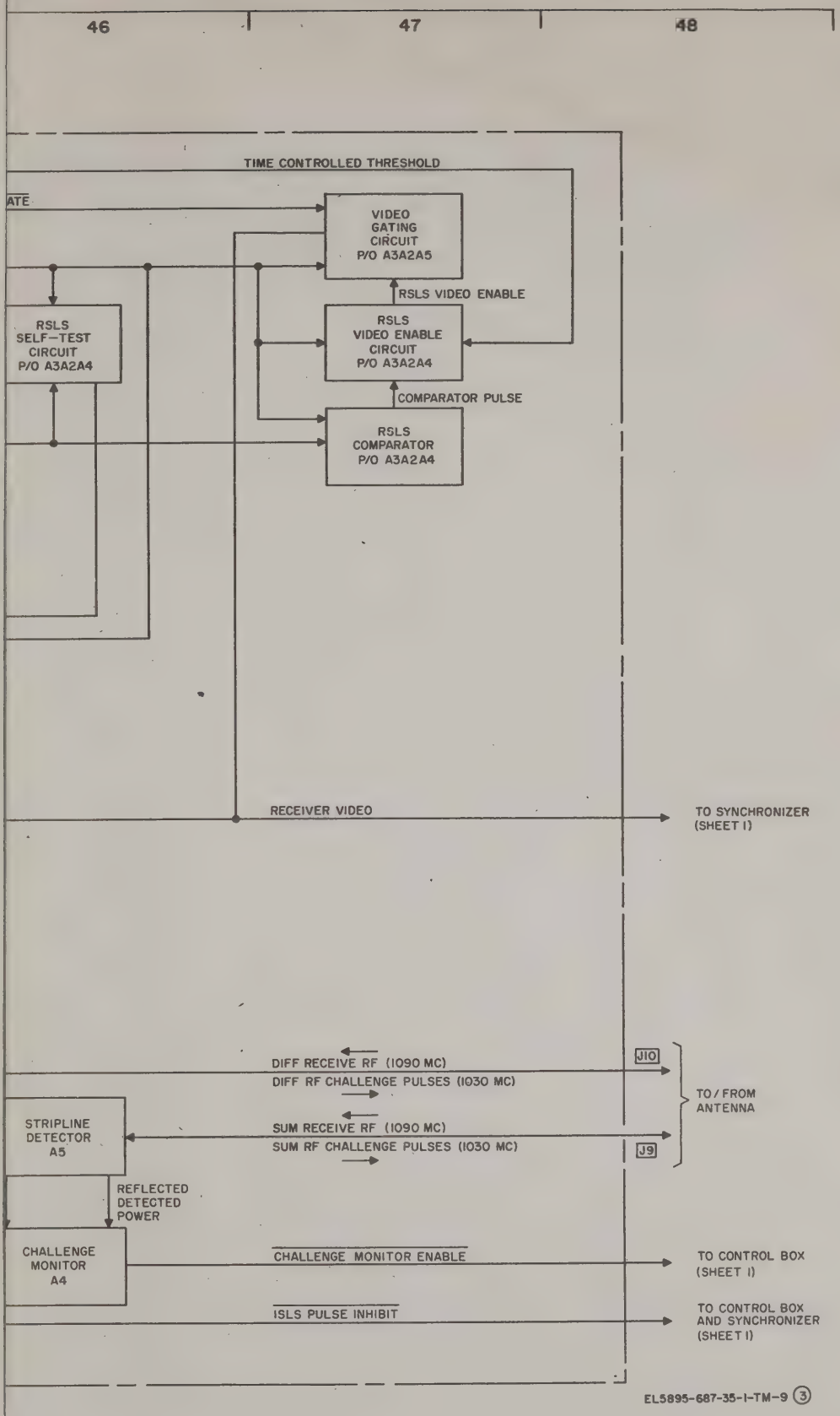


Figure 12-2(2). IFF set, system functional block diagram (sheet 2 of 3).


46
47
48
TIME CONTROLLED THRESHOLD
ATE
VIDEO GATING CIRCUIT P/O A3A2A5
RSLS VIDEO ENABLE
RSLS SELF-TEST CIRCUIT P/O A3A2A4
RSLS VIDEO ENABLE CIRCUIT P/O A3A2A4
COMPARATOR PULSE
RSLS COMPARATOR P/O A3A2A4
RECEIVER VIDEO
TO SYNCHRONIZER (SHEET 1)
DIFF RECEIVE RF (1090 MC)
DIFF RF CHALLENGE PULSES (1030 MC)
J10
TO/FROM ANTENNA
STRIPLINE DETECTOR A5
SUM RECEIVE RF (1090 MC)
SUM RF CHALLENGE PULSES (1030 MC)
J9
REFLECTED DETECTED POWER
CHALLENGE MONITOR A4
CHALLENGE MONITOR ENABLE
TO CONTROL BOX (SHEET 1)
ISLS PULSE INHIBIT
TO CONTROL BOX AND SYNCHRONIZER (SHEET 1)
EL5895-687-35-1-TM-9 (3)

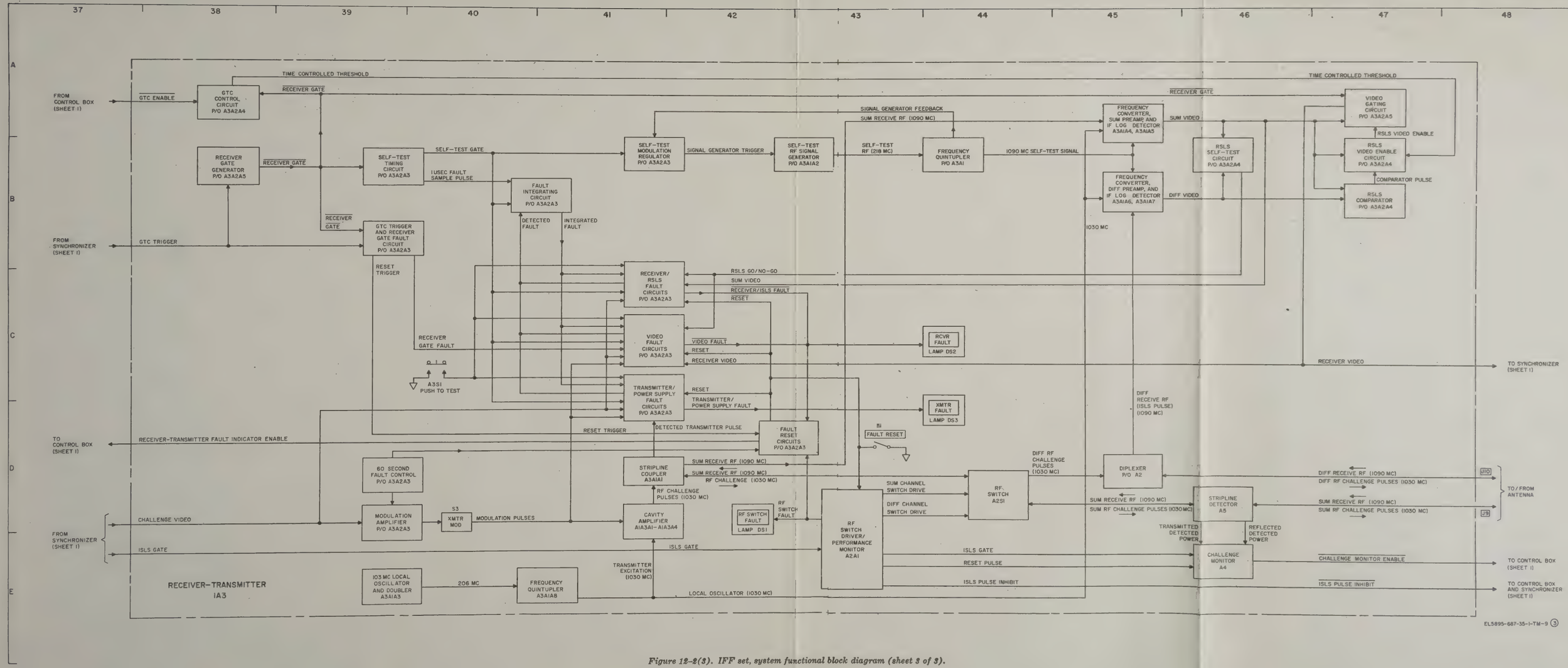
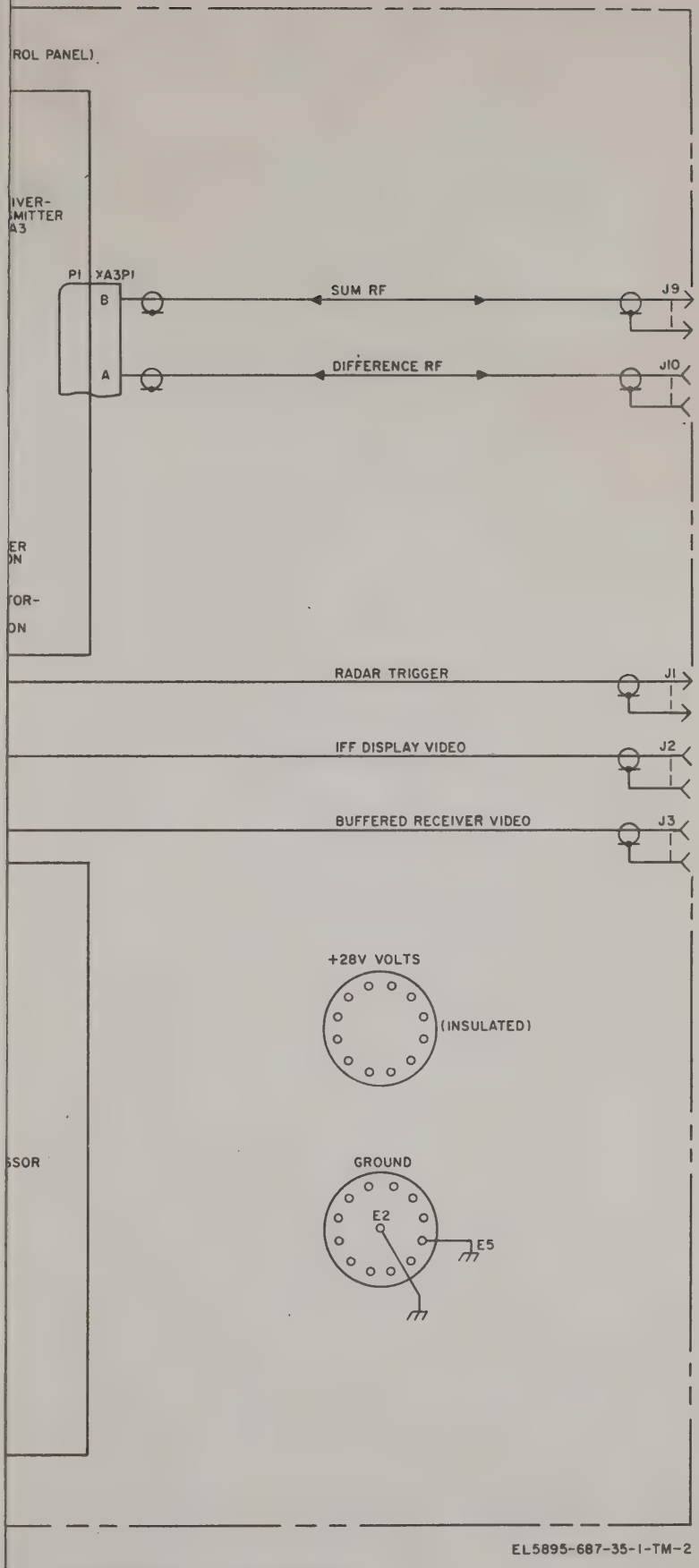


Figure 12-2(3). IFF set, system functional block diagram (sheet 3 of 3).



set, interconnection wiring diagram.

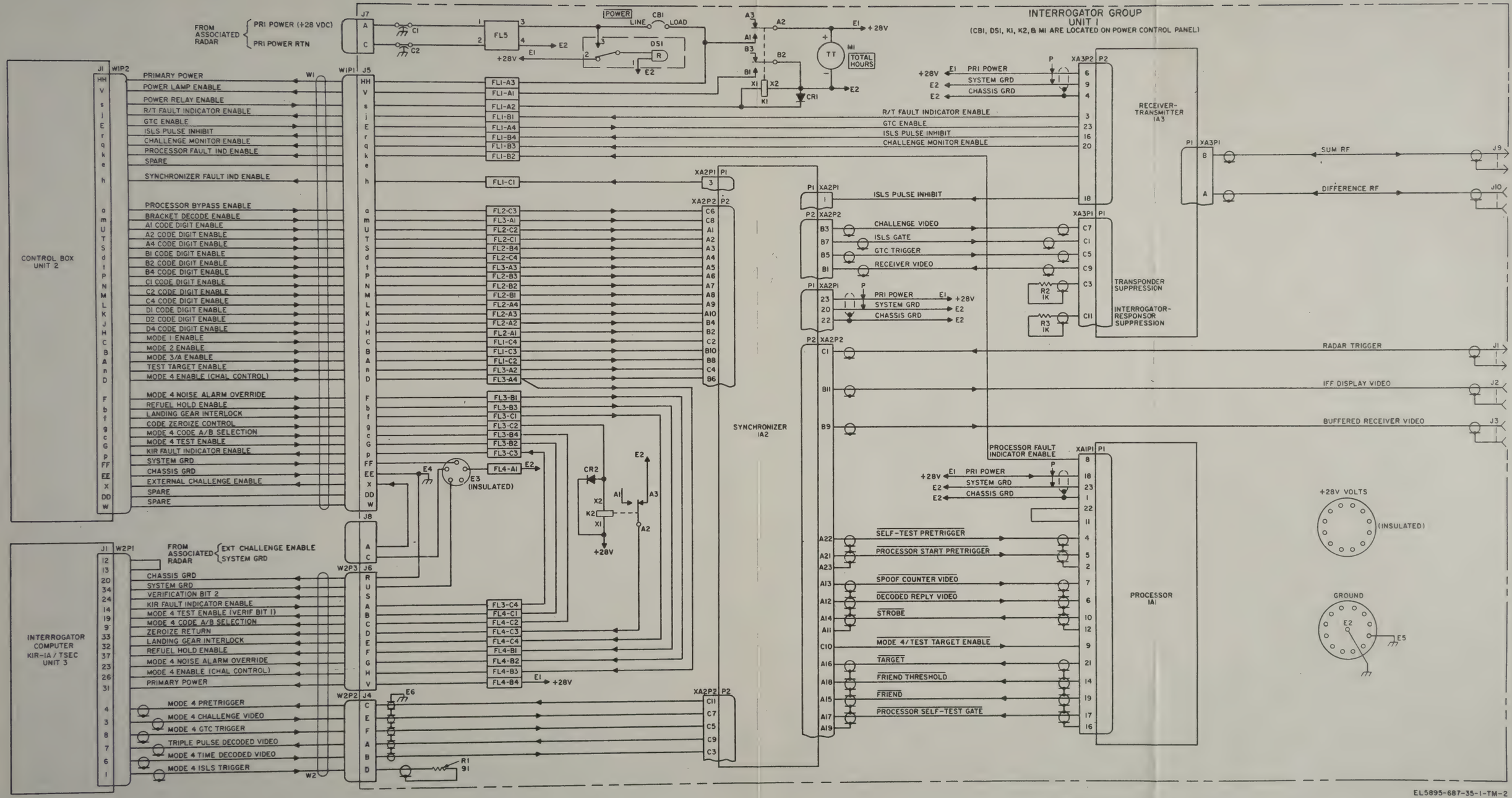
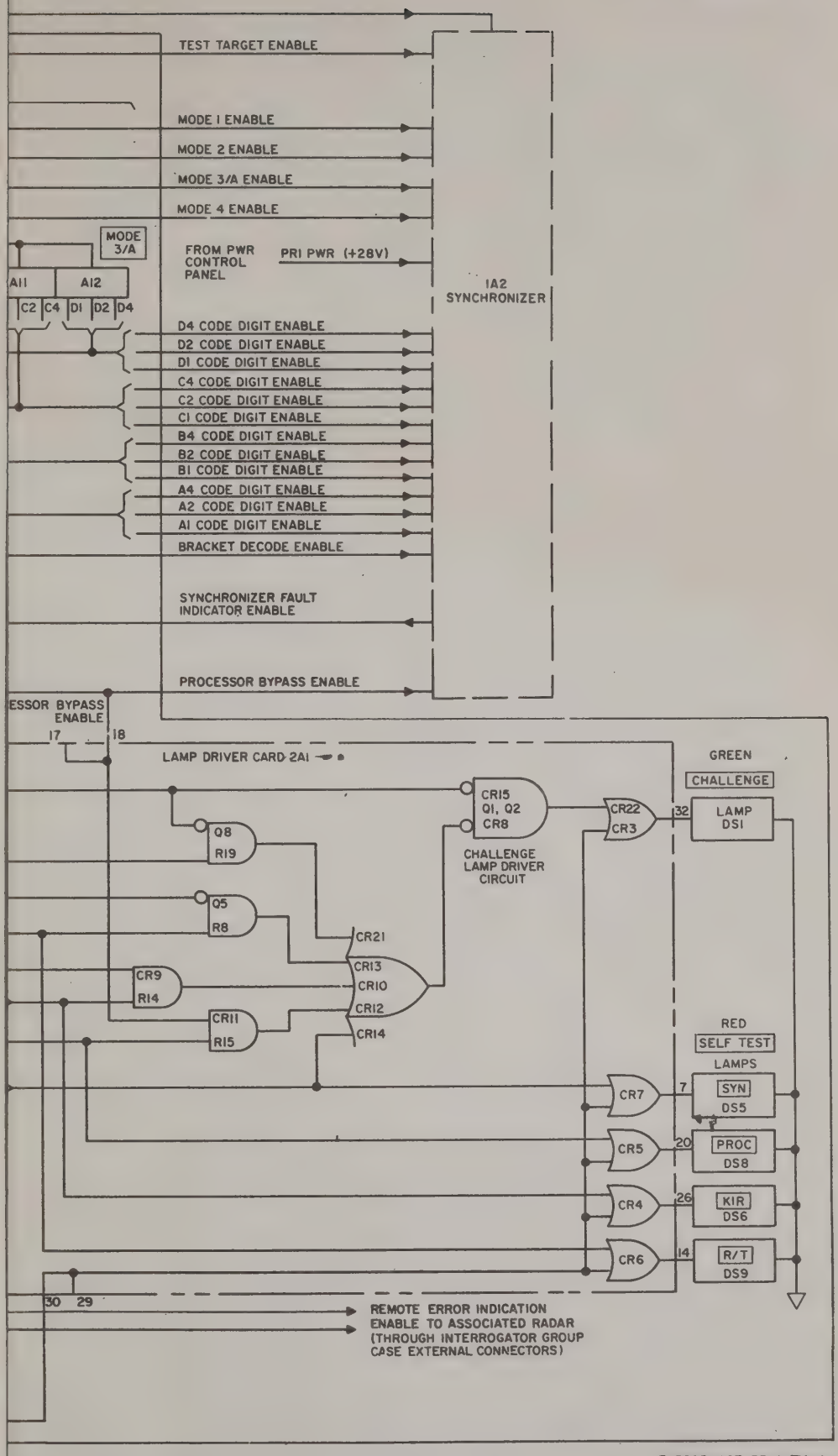


Figure 12–3. IFF set, interconnection wiring diagram.



EL5895-687-35-1-TM-4

Figure 12–4. Control circuits, functional block diagram.

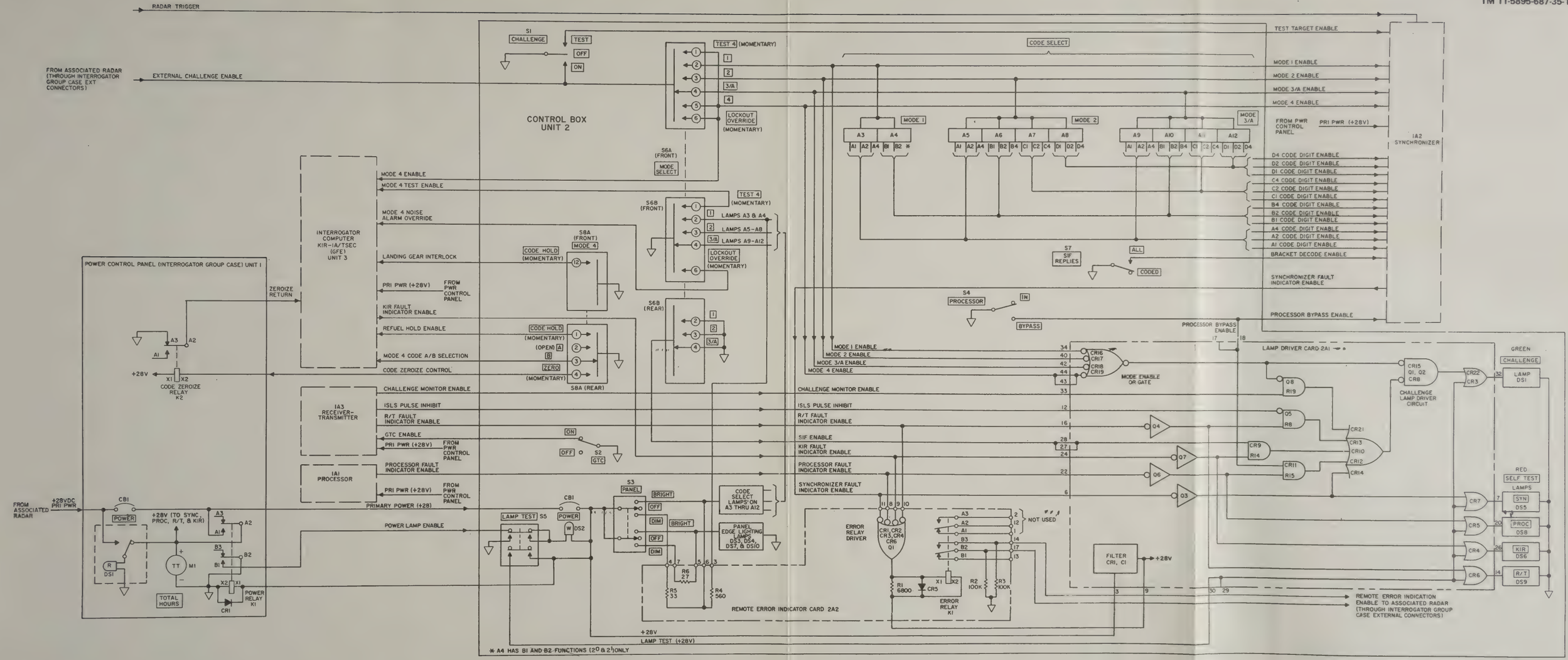
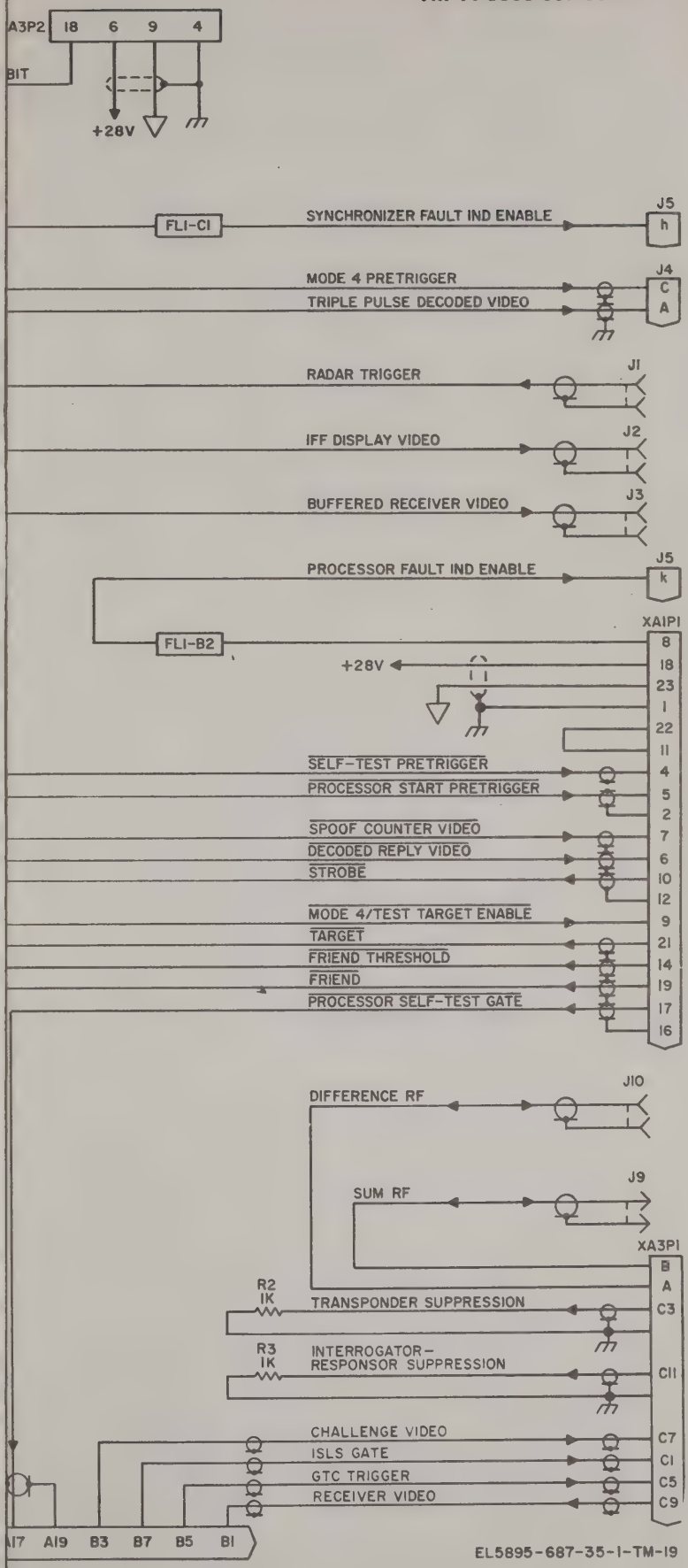


Figure 12-4. Control circuits, functional block diagram.



group case unit 1, schematic diagram.

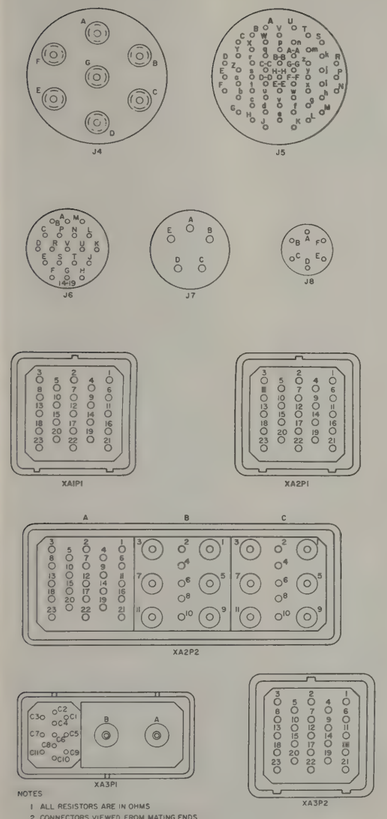
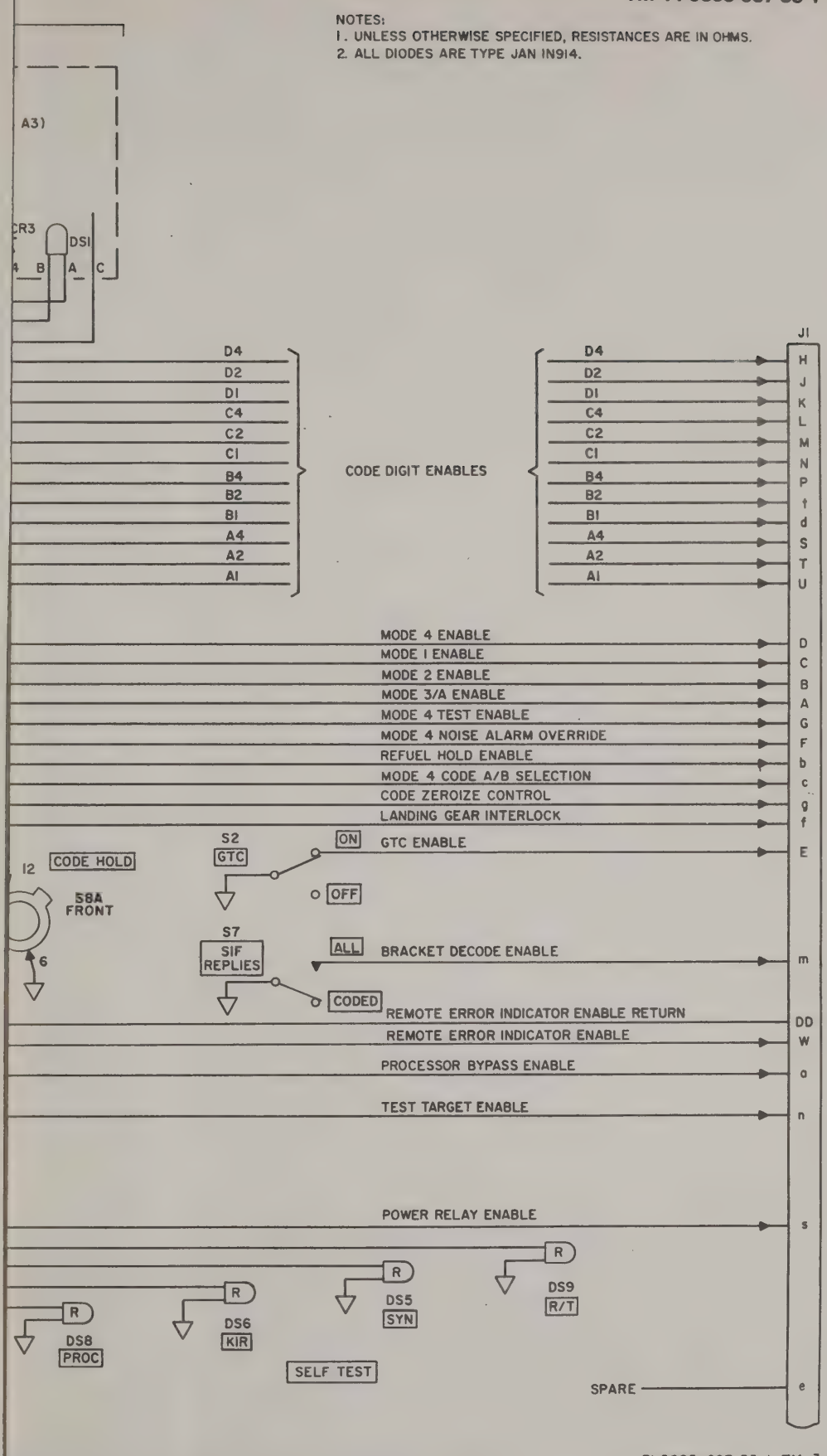


Figure 12-5. Interrogator group case unit 1, schematic diagram.



EL5895-687-35-1-TM-3

Figure 12–6. Control box, interconnection block diagram.

NOTES:
1. UNLESS OTHERWISE SPECIFIED, RESISTANCES ARE IN OHMS.
2. ALL DIODES ARE TYPE JAN IN914.

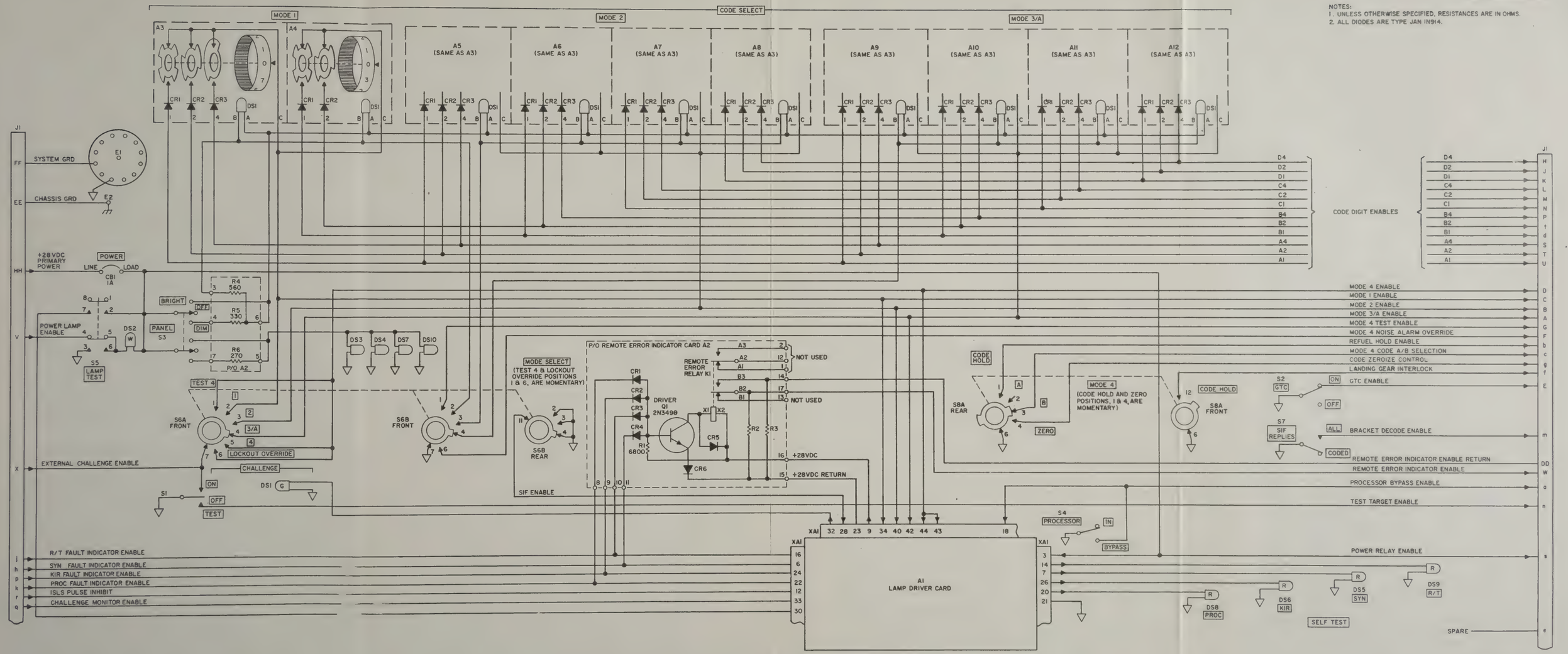
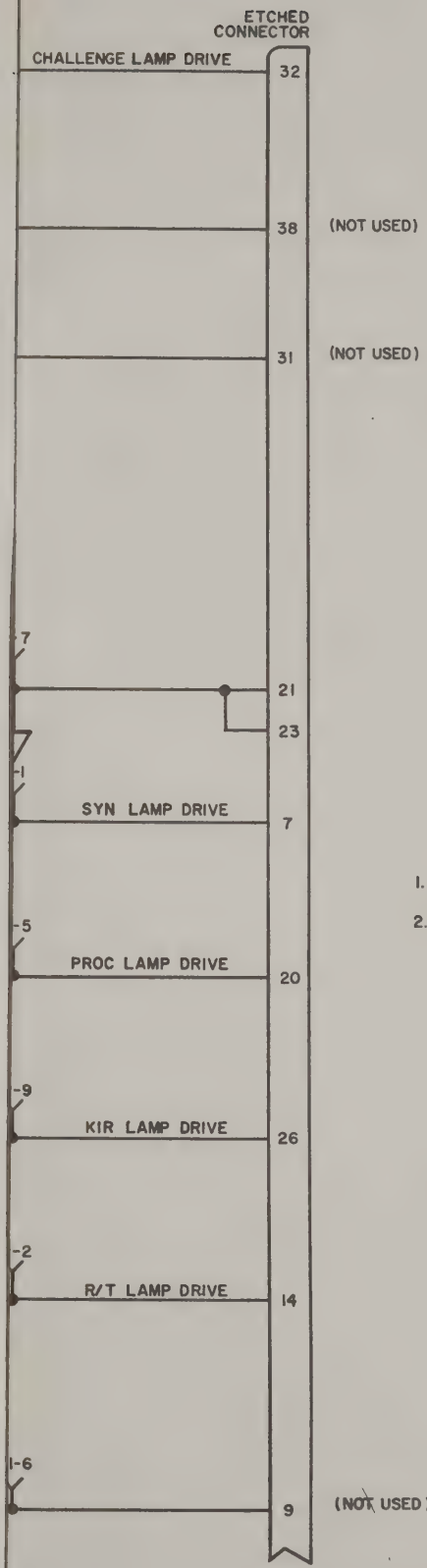


Figure 12–6. Control box, interconnection block diagram.

EL5895-687-35-1-TM-3

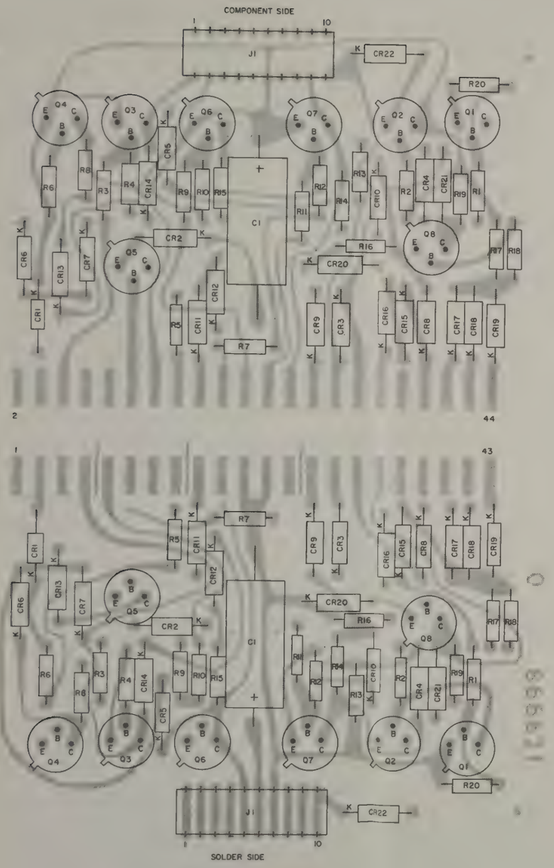


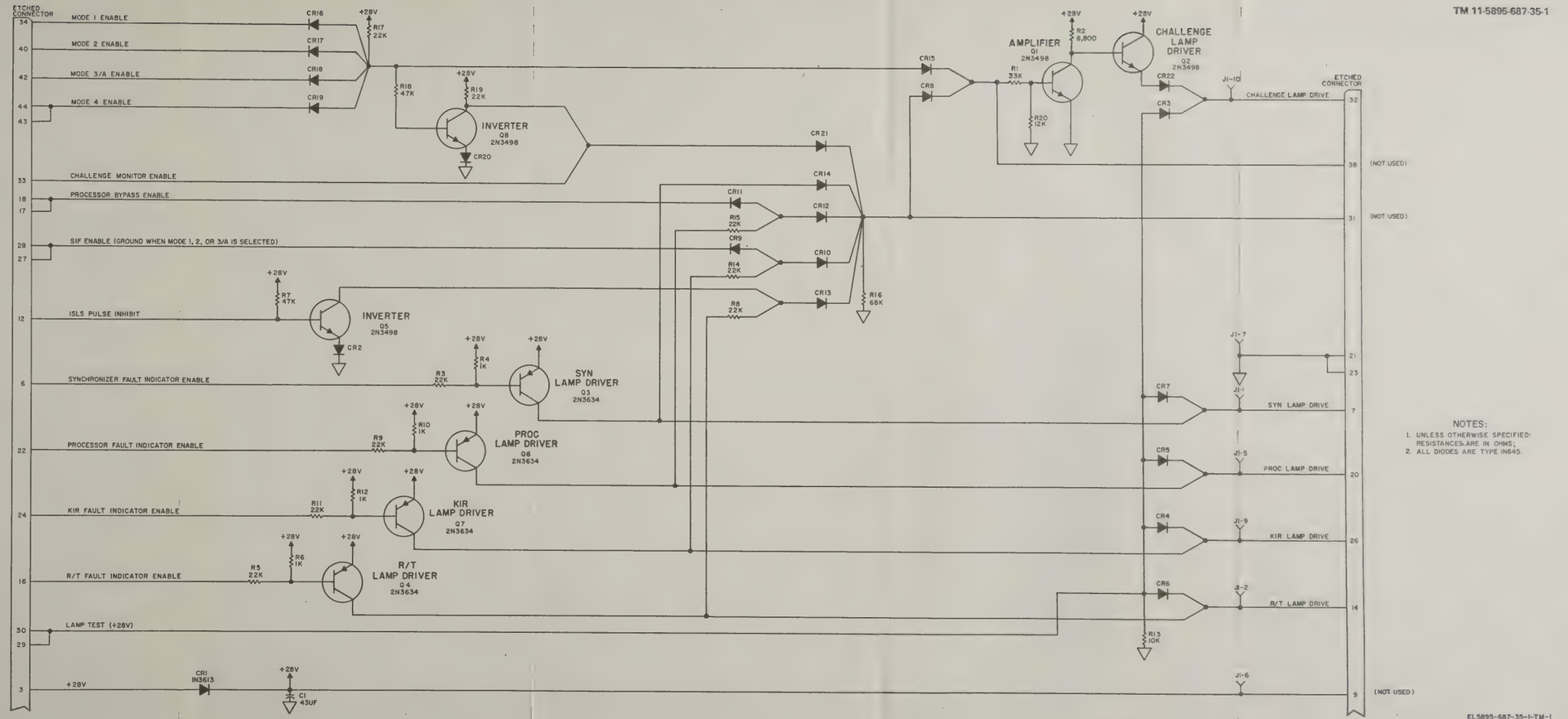
NOTES:

1. UNLESS OTHERWISE SPECIFIED: RESISTANCES ARE IN OHMS;
2. ALL DIODES ARE TYPE IN645.

EL5895-687-35-1-TM-1

2A1, schematic diagram and component locations.





NOTES:
1. UNLESS OTHERWISE SPECIFIED: RESISTANCES ARE IN OHMS;
2. ALL DIODES ARE TYPE IN645.

EL5895-687-35-1-TM-1

Figure 12-7. Lamp driver card 2A1, schematic diagram and component locations.

APPENDIX

REFERENCES

The following is a list of references applicable and available to the direct support, general support and depot maintenance repairman of Interrogator Set AN/TPX–50.

T.O. 33A1–8–468–1/ TM 11–6625–1711–15/ NAVAIR 16–30–APM245–1	Test Set AN/APM–245
TM 9–4940–465–12	Heat Gun, Master Appliance Model HG–501L
TM 11–5109	Slotted Line, Coaxial IM–92/U
TM 11–6130–245–15	Power Supply PP–2309 A/U
TM 11–6625–280–15	Generator, Signal AN/URM–49
TM 11–6625–299–15	Generator, Signal AN/URM–64
TM 11–6625–335–12	Indicator, Standing Wave, Ratio AN/UPM–108A
TM 11–6625–403–14	Test Set AN/UPM–98
TM 11–6625–433–15	Wattmeter AN/URM–98
TM 11–6625–535–15	Oscilloscope AN/USM–140A
TM 11–6625–700–10	Counter, Electronic, Digital Readout AN/USM–207
TM 11–6625–1338–50	Voltmeter, Electronic, ME–202A/U
TM 11–6625–1559–12	Generator, Service Signal AN/USM–203
TM 11–6625–2398–15–3	Test Facilities Set AN/TPM–24 (V) 3

INDEX

	Paragraph	Page
Additional test equipment required	5–27	5–20
Adjustment and alignment procedures	9–2	9–1
AND gate circuits	2–4	2–1
AN/TPX–50 diode resistances	5–6	5–2
Bench servicing connections:		
Control box	7–15	7–12
Interrogator group case	7–11	7–8
Bench troubleshooting:		
Control box	7–16	7–12
Interrogator group case	7–12	7–8
Cabinet, Interrogator Set Group CY–6442/TPX–50 resistances	5–8	5–5
Cable check and repair	5–16	5–8
Challenge encoding	3–4*a*	3–4
Challenge encoding circuit self-test	3–6*a*(2)	3–10
CHALLENGE lamp driver	4–11	4–7
CHALLENGE lamp DS1	4–10	4–7
CHALLENGE switch S1	4–6*b*	4–3
Challenge transmitting	3–4*c*	3–5
Challenging	3–4	3–4
Challenging:		
Mode 1	4–6*f*	4–5
Mode 2	4–6*g*	4–5
Mode 3	4–6*h*	4–5
Mode 4	4–7	4–5
Challenging in mode 4	4–7	4–5
Challenging in the sif modes	4–6	4–3
Checking serviceability	5–1*e*	5–2
CODE SELECT switch assemblies	4–6*b*	4–3
Complete alignment and testing of AN/TPX–50, general	9–1	9–1
Confidence checks	4–6	4–3
Control box:		
Bench servicing connections	7–15	7–12
Bench troubleshooting	7–16	7–12
Removal and replacement of parts	7–17	7–12
Control circuit functioning, general	4–1	4–1
Control circuits	4–2	4–1
Control circuits, controls and functions	7–2	7–1
Control circuits testing:		
Equipment	7–8	7–7
General	7–7	7–7
Testing procedure	7–9	7–7
Control circuit troubleshooting and repair:		
Reference data	7–1	7–1
Control circuits troubleshooting:		
Chart	7–6	7–5
General	7–3	7–4
Preparation	7–5	7–5
Test equipment	7–4	7–4
Control, Interrogator Set C–7651/TPX–50 resistances	5–7	5–4
Control settings, preliminary checks and	6–3	6–1
Correcting trouble	5–1*d*	5–1
Decoding circuits	3–5*b*	3–6
Detecting faulty operation	5–1*b*	5–1
Diode resistances	5–6	5–3
Display video circuits self-test	3–6*a*(4)	3–11
Error indicator drivers	3–6*c*(4)	3–14

	Paragraph	Page
Fault indicator enable lines:		
KIR	4–18	4–9
Processor	4–16	4–8
R/T	4–17	4–9
Synchronizer	4–15	4–8
Fuses and interlocks	6–3	6–1
General information	1–3	1–1
General maintenance information, purpose	5–1	5–1
General support testing procedures:		
Additional equipments	10–6*a*	10–3
General	10–1	10–1
Initial IFF set control settings	10–6*e*	10–4
Initial test equipment control settings	10–6*f*	10–4
Physical test and inspection	10–5	10–2
Test connections	10–6*c*	10–4
Test equipment	10–2	10–1
Test facilities	10–3	10–1
Test procedures	10–6	10–3
Graphic symbols	1–3*c*	1–1
GTC switch S2	4–6*e*	4–4
Hot mockup of the IFF set	5–25	5–17
IFF display video	3–5*d*	3–9
IFF system functioning:		
General	3–1	3–1
Timing circuits	3–2	3–1
Indexes of publications	1–2	1–1
Interlocks, fuses and	6–3	6–1
Intermittents	5–19	5–13
Introduction	1–1	1–1
Inverter circuit	2–3	2–1
Isls timing	3–4*b*	3–4
KIR fault indicator enable line	4–18	4–9
Lamp driver card 2A1	4–9	4–7
Lamp driver card 2A1, reference data	8–1	8–1
Lamp driver card 2A1, symptom troubleshooting	8–2	8–1
Lamp driver card 2A1 symptom troubleshooting chart	8–5	8–1
Lamp driver card 2A1, voltage and resistance measurement	8–6	8–4
Lamp drivers:		
CHALLENGE	4–11	4–7
SELF TEST	4–13	4–8
LAMP TEST pushbutton switch S1	4–4*a*	4–2
Locating trouble	5–1*c*	5–1
Logic symbols:	2–2	2–1
AND gate circuits	2–4	2–1
OR gate circuits	2–5	2–2
Inverter circuit	2–3	2–1
Mode enable and challenge monitor enable lines	4–14	4–8
MODE SELECT switch S6	4–6*a*, 4–7*a*	4–3, 4–5
Mode switching	3–3	3–2
Mode 4 challenge encoding	3–4*a*(2)	3–4
Mode 1 challenging	4–6*f*	4–5
Mode 2 challenging	4–6*g*	4–5
Mode 3/A challenging	4–6*h*	4–5
Mode 4 challenging	4–7	4–5
Mode 4 decoding	3–5*b*(2)	3–7
Mode 4 switching	3–3*b*	3–2
MODE 4 switch S8	4–7*b*	4–6
Modification work orders	10–4	10–2
OR gate circuits	2–5	2–2

	Paragraph	Page
Parts location	5–10	5–6
Parts substitution	5–15	5–8
Physical test and inspection gs support testing procedures	10–5	10–2
Power short circuits	5–20	5–13
Preliminary checks and control settings	6–4	6–1
Preparation for troubleshooting control circuits	7–5	7–5
Preparation of lamp driver card 2A1 for troubleshooting	8–4	8–1
Preparing to challenge	4–5	4–3
Pretrigger generation	3–2*b*	3–1
Pretriggers:		
Mode 4	3–2*b*(1)	3–1
Processor start	3–2*b*(4)	3–2
Self-test	3–2*b*(2)	3–1
Sif	3–2*b*(3)	3–2
Processor bypass switching	3–3*d*	3–3
Processor fault indicator enable line	4–16	4–8
Processor self-test circuits and fault indicators	3–6*c*	3–13
PROCESSOR switch S4	4–6*d*	4–4
Radar trigger	3–2*a*	3–1
Receiving circuits	3–5*a*	3–5
Receiving circuit self-test	3–6*b*(2)	3–12
Receiver transmitter self-test circuits and fault indicators	3–6*b*	3–11
Reference data	6–2	6–1
Reference data, control circuit troubleshooting	7–1	7–1
Reference data, lamp driver card 2A1	8–1	8–1
Reference designation number location chart	5–9	5–5
Remote error indicator card	4–19	4–10
Removal and replacement of conformal coating	5–22	5–15
Removal and replacement of parts:		
Control box	7–17	7–12
Interrogator group case	7–13	7–8
Repair of cables W1 and W2	5–17	5–9
Repair of coaxial cable RG–180	5–18	5–11
Repair of printing wiring	5–24	5–16
Replacing integrated circuits	5–13	5–7
Replacing modules	5–11	5–6
Replacing piece parts	5–14	5–7
Replacing printed wiring cards	5–12	5–6
Reply decoding	3–5	3–5
Reply decoding circuits self-test	3–6*a*(3)	3–11
Reply processing	3–5*c*	3–7
Resistances, control box	5–7	5–4
Resistances, interrogator group case	5–8	5–5
R/T fault indicator enable line	4–17	4–9
Scope of manual	1–1	1–1
Self-test circuits and fault indicators:	3–6	3–10
Processor	3–6*c*	3–13
Receiver transmitter	3–6*b*	3–11
Synchronizer	3–6*a*	3–10
Self-test cycle counter and decoders	3–6*c*(2)	3–13
SELF TEST lamp drivers	4–13	4–8
SELF TEST lamps	4–12	4–7
Self-test reply and error gates	3–6*c*(3)	3–13
Sif challenge encoding	3–4*a*(1)	3–4
Sif decoding	3–5*b*(1)	3–6
Sif mode switching	3–3*a*	3–2
Sif replies switching	3–3*c*	3–3
SIF REPLIES switch S7	4–6*c*	4–4
Soldering techniques	5–23	5–15
Summary of test data	10–7	10–26

	Paragraph	Page
Switching:		
Mode	3–3	3–2
Sif	3–3a	3–2
Mode 4	3–3*b*	3–2
Sif replies	3–3*c*	3–3
Processor bypass	3–3*d*	3–3
Symptom troubleshooting, lamp driver card 2A1	8–2	8–1
Synchronizer fault indicator enable	4–15	4–8
Synchronizer self-test circuits and fault indicators	3–6*a*	3–10
Test data, summary	10–7	10–26
Test equipments, gs testing procedures	10–2	10–1
Test equipment required, lamp driver card 2A1	8–3	8–1
Test equipment required to troubleshoot control circuits	7–4	7–4
Test facilities, gs testing procedures	10–3	10–1
Test procedures	9–3	9–1
Test target mode	3–7	3–14
Testing control circuits:		
Equipment required	7–8	7–7
General	7–7	7–7
Procedure	7–9	7–7
Testing procedures, general support	10–6	10–3
Theory of similar functions, general	2–1	2–1
Timing circuits self-test	3–6*a*(1)	3–10
Timing error detector	3–6*c*(1)	3–13
Tools required	5–26	5–20
Transistor testing	5–21	5–14
Transmitting circuit self-test	3–6*b*(1)	3–1
Troubleshooting and repair of interrogator group case	7–10	7–77
Bench servicing and connections	7–11	7–8
Bench troubleshooting	7–12	7–8
Removal and replacement of parts	7–13	7–8
Troubleshooting based on starting procedure	6–5	6–7
Troubleshooting based on starting procedure, general	6–1	6–1
Troubleshooting data	5–3	5–2
Troubleshooting reference data	6–2	6–1
Troubleshooting techniques	5–2	5–2
Turning off the IFF set	4–8	4–7
Turning on the IFF set	4–3	4–1
Voltage and resistance measurements	5–5	5–3
Voltage and resistance measurements, lamp driver card 2A1	8–6	8–4
Waveform analysis	5–4	5–3

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